MU182020A 25 Gbit/s 1ch MUX MU182021A 25 Gbit/s 2ch MUX Operation Manual

Eighth Edition

- For safety and warning information, please read this manual before attempting to use the equipment.
- Additional safety and warning information is provided in the MP1800A Signal Quality Analyzer Installation Guide and the MT1810A 4 Slot Chassis Installation Guide. Please also refer to one of these documents before using the equipment.
- Keep this manual with the equipment.

ANRITSU CORPORATION

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This indicates a prohibited operation. The prohibited operation is indicated symbolically in or near the barred circle.

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This indicates a warning or caution. The contents are indicated symbolically in or near the triangle.

This indicates a note. The contents are described in the box.

These indicate that the marked part should be recycled.

MU182020A 25 Gbit/s 1ch MUX MU182021A 25 Gbit/s 2ch MUX Operation Manual

- 30 September 2008 (First Edition)
- 20 June 2013 (Eighth Edition)

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- In places where high-intensity static electric charges or electromagnetic fields are present
- In places where abnormal power voltages (high or low) or instantaneous power failures occur
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CE marking

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1. Product Model

Plug-in Units:

MU182020A 25 Gbit/s 1ch MUX MU182021A 25 Gbit/s 2ch MUX

2. Applied Directive and Standards

When the MU182020A 25 Gbit/s 1ch MUX or MU182021A 25 Gbit/s 2ch MUX is installed in the MP1800A or MT1810A, the applied directive and standards of this unit conform to those of the MP1800A or MT1810A main frame.

PS: About main frame

Please contact Anritsu for the latest information on the main frame types that MU182020A/21A can be used with.

C-Tick Conformity Marking

Anritsu affixes the C-Tick marking on the following product(s) in accordance with the regulation to indicate that they conform to the EMC framework of Australia/New Zealand.

C-Tick marking



1. Product Model

Plug-in Units:

MU182020A 25 Gbit/s 1ch MUX MU182021A 25 Gbit/s 2ch MUX

2. Applied Directive and Standards

When the MU182020A 25 Gbit/s 1ch MUX or MU182021A 25 Gbit/s 2ch MUX is installed in the MP1800A or MT1810A, the applied directive and standards of this unit conform to those of the MP1800A or MT1810A main frame.

PS: About main frame

Please contact Anritsu for the latest information on the main frame types that MU182020A/21A can be used with.

About This Manual

A testing system combining an MP1800A Signal Quality Analyzer or MT1810A 4-Slot Chassis mainframe, module(s), and control software is called a Signal Quality Analyzer Series. The operation manuals of the Signal Quality Analyzer Series consist of separate documents for the installation guide, the mainframe, remote control operation, module(s), and control software, as shown below.



Operation manual of the software that controls the Signal Quality Analyzer Series.

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This chapter provides an overview of the MU182020A 25 Gbit/s 1ch MUX and MU182021A 25 Gbit/s 2ch MUX (hereinafter, referred to as "MU182020A/21A").

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1.1 Product Overview

The MU182020A/21A is a plug-in module that can be built into a Signal Quality Analyzer mainframe. This equipment 2:1 multiplexes the output signal of the MU181020A 12.5 Gbit/s and MU181020B 14 Gbit/s pulse pattern generators (hereafter MU181020A/B) to generate 8 to 25 Gbit/s PRBS, DATA and Zero-Substitution patterns.

Various option configurations are available for the MU181020A. This module is therefore useful for research, development, and production of various types of digital communication equipment, modules, and devices.

Features of the MU182020A/21A:

- Operating rates: 8 to 25 Gbit/s (28 Gbit/s using additional options)
- Multiplexes input data signal to 2:1 (MU182020A) or 4:2 (MU182021A)
- High-quality output signal waveform
- Flexible for functional expansion in the future, by installing additional options.

1.2 Product Composition

1.2.1 Standard composition

Table 1.2.1-1 and Table 1.2.1-2 show the standard composition for the MU182020A/21A.

ltem	Model name/symbol	Product name	Q'ty	Remarks
Mainframe	MU182020A	25 Gbit/s 1ch MUX	1	
	J1137	Coaxial Terminator	5	
	J1341A	Open	4	
	J1359A	Coaxial Adapter (K-P, K-J, SMA compatibility)	2	
Accessory	Z0897A	MP1800A Manual CD	1	CD-ROM version
1100055017	Z0918A	MX180000A Software CD	1	CD-ROM version
	J1427A	Cable kit for 20A/40A (Tx/Rx ,Opt16)	1	Either J1427A or
	J1448A	Cable kit for 20A/40A (Tx/Rx ,Opt15)		J1448A is attached, depending on the options used.

Table 1.2.1-2	Standard composition for MU1820	21A
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ltem	Model name/symbol	Product name		Remarks
Mainframe	MU182021A	25 Gbit/s 2ch MUX		
	J1137	Coaxial Terminator	9	
	J1341A	Open	6	
Accessory	J1359A	Coaxial Adapter (K-P, K-J, SMA compatibility)	4	
	Z0897A	MP1800A Manual CD	1	CD-ROM version
	Z0918A	MX180000A Software CD	1	CD-ROM version
	J1428A	Cable kit for 21A (Tx ,Opt15/16)	1	

1.2.2 Options

Table 1.2.2-1 and Table 1.2.2-2 show the options for the MU182020A/21A.Table 1.2.2-3 and Table 1.2.2-4 show the accessories for theMU182020A/21A.All options are sold separately.

Model name	Product name	Remarks
MU182020A-x01	28 Gbit/s Extension	
MU182020A-x02	Clock Input Band Switch	
MU182020A-x03*	28.1 Gbit/s Extension	Can be installed together with MU182020A-x01.
MU182020A-x10	Variable Data Output (0.25 to 1.75 Vp-p) Retrofit	Cannot be installed together with MU182020A-x11 and MU182020A-x13.
MU182020A-x11	Variable Data Output (0.5 to 2.5 Vp-p) Retrofit	Cannot be installed together with MU182020A-x10 and MU182020A-x13.
MU182020A-x13	Variable Data Output (0.5 to 3.5 Vp-p) Retrofit	Cannot be installed together with MU182020A-x10 and MU182020A-x11.
MU182020A-x21	Variable Clock Output (0.5 to 2.0 Vp-p)	
MU182020A-x30	25Gbit/s Variable Data Delay	Cannot be installed together with MU182020A-x31.
MU182020A-x31	28Gbit/s Variable Data Delay	Cannot be installed together with MU182020A-x30.

Table 1.2.2-1 Options for MU182020A

Table 1.2.2-2	Options for MU ²	182021A
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Model name	Product name	Remarks
MU182021A-x01	28 Gbit/s Extension	
MU182021A-x02	Clock Input Band Switch	
MU182021A-x03*	28.1 Gbit/s Extension	Can be installed together with MU182021A-x01.
MU182021A-x10	Variable Data Output (0.25 to 1.75 Vp-p) Retrofit	Cannot be installed together with MU182021A-x11 and MU182021A-x13.
MU182021A-x11	Variable Data Output (0.5 to 2.5 Vp-p) Retrofit	Cannot be installed together with MU182021A-x10 and MU182021A-x13.
MU182021A-x13	Variable Data Output (0.5 to 3.5 Vp-p) Retrofit	Cannot be installed together with MU182021A-x10 and MU182021A-x11.
MU182021A-x21	Differential Clock Output (0.5 to 2.0Vp-p)	
MU182021A-x30	25Gbit/s Variable Data Delay	Cannot be installed together with MU182021A-x31.
MU182021A-x31	28Gbit/s Variable Data Delay	Cannot be installed together with MU182021A-x30.
MU182021A-x40	Emphasis Control	

*: Notice of MU182020A/21A-x03 option name indication

Option name of MU182020A-x01+x03, or MU182021A-x01+x03 is indicated on the module ejector. On option display of the software, it is displayed as "MU182020A/21A-x01(28Gbit/s Extension)". However, the operation between 8.0 to 28.1 Gbit/s bit rate is guaranteed.

Note:

Option name format is as follows:



Target Option	Model name/symbol	Product name	Q'ty	Remarks
MU182020A-x02	J1359A	Coaxial Adapter (K-P, K-J, SMA compatibility)	2	
MU182020A-x21	J1359A	Coaxial Adapter (K-P, K-J, SMA compatibility)	1	

Table 1.2.2-4	MU182021A	options and	accessories
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Target Option	Model name/symbol	Product name	Q'ty	Remarks
MU182021A-x02	J1359A	Coaxial Adapter (K-P, K-J, SMA compatibility)	2	
MU182021A-x21	J1137	Coaxial Terminator	1	
	J1359A	Coaxial Adapter (K-P, K-J, SMA compatibility)	2	

1.2.3 Application parts

Table 1.2.3-1 shows the application parts for the MU182020A/21A. All application parts are sold separately.

Model name/ symbol	Product name	Remarks
J1137	Terminator	SMA-P
J1342A	Coaxial cable 0.8m	APC 3.5 connector
J1343A	Coaxial cable 1M	SMA connector
J1359A	Coaxial adaptor (K-P.K-J,SMA)	
J1427A	Cable kit for 20A/40A (Tx/Rx ,Opt16)	1/2 Data Input×2 (TX) 1/2 Clock Input×1 (TX) 1/2 Clock Output×2 (TX) 1/2 Data Output×2 (RX) 1/2 Clock Output×2 (RX)
J1428A	Cable kit for 21A (Tx ,Opt15/16)	1/2 Data Input×4 1/2 Clock Input×1 1/2 Clock Output×4
J1439A	Coaxial cable (0.8m, K connector)	K connector
J1448A	Cable kit for 20A/40A (Tx/Rx ,Opt15)	1/2 Data Input×2 (TX) 1/2 Clock Input×1 (TX) 1/2 Clock Output×2 (TX) 1/2 Data Output×2 (RX) 1/2 Clock Output×2 (RX)
J1449A	Measurement kit (K connector)	Coaxial cable (0.8m, K connector) $\times 2$ Coaxial cable 0.8 m $\times 2$ Coaxial cable 1 m $\times 1$
J1450A	Coaxial attenuator	41KC-3
J1451A	Coaxial attenuator	41KC-6
J1452A	Coaxial attenuator	41KC-10
J1453A	Coaxial attenuator	41KC-20
J1454A	Power Divider	K240C
W3128AW	MU182020A/MU182021A Operation Manual	Printed version

Table 1.2.3-1 Application parts

1.3 Specifications

1.3.1 Specifications for MU182020A

Table 1.3.1-1	Specifications for MU182020A
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ltem		Specifications	Remarks
Operating bit rate)	8.0 to 25.0 Gbit/s 8.0 to 28.0 Gbit/s (When MU182020A-x01 is installed) 8.0 to 28.1 Gbit/s (When MU182020A-x01 ,x03 installed)	
External clock input	Number of Input	1	
(from System Clock)	Frequency	4.0 to 12.5 GHz 4.0 to 14.0 GHz (When MU182020A-x01 is installed) 4.0 to 14.05 GHz (When MU182020A-x01, x03 installed)	
		4.0 to 12.5 GHz 8.0 to 25.0 GHz (switchable when MU182020A-x02 installed)	
		4.0 to 14.0 GHz 8.0 to 28.0 GHz (switchable when MU182020A-x01, x02 installed)	
		4.0 to 14.05 GHz 8.0 to 28.1 GHz (switchable when MU182020A-x01, x02 ,x03 installed)	
	Amplitude	0.3 to 1.0 Vp-p	
	Termination	ΑC/50 Ω	
	Connector	SMA (when MU182020A-x02 is not installed) K (when MU182020A-x02 installed)	
1/2 Data Input	Number of Input	2 (1/2 Data Input A,1/2 Data Input B)	From MU181020A/B
	Level	0/-1 V H:-0.25 to +0.05 V L:-1.4 to -0.85 V	Data Output
	Termination	50 Ω/GND	
	Connector	SMA	

Item		Specifications	Remarks
1/2 Clock Input	Number of Input	1	From MU181020A/B
	Amplitude	0.25 to 1.0 Vp-p	Clock Output
	Termination	ΑC/50 Ω	
	Connector	SMA	
	Amplitude	Min. 0.4 Vp-p, Max. 1.2 Vp-p	
	Termination	ΑC/50 Ω	
1/2 Clock	Clock Output	2	То
Output	Amplitude	Min. 0.4 Vp-p, Max. 1.2 Vp-p	MU181020A/B
	Termination	ΑC/50 Ω	Ext Clock Input
	Connector	SMA	
	Between channels Skew	≤10 ps 12 GHz (when MU182020A-x01 uninstalled) 14 GHz (whenMU182020A-x01 installed) 14.05 GHz (whenMU182020A-x01+x03 installed)	

Table 1.3.1-1 Specifications for MU182020A (Cont'd)

ltem		Specifications	Remarks
Data Output*1 MU182020A-	Number of Output	$2 \left(\text{Data} / \overline{\text{Data}} \right)$	$\begin{array}{llllllllllllllllllllllllllllllllllll$
x10 (Variable Data	Amplitude	0.25 to 1.75 Vp-p/2 mV Step (Independent, variable)	Mark Ratio 1/2
Output (0.25 to 1.75 Vp-p))		Accuracy:±50 mV ±17% of Amplitude (Cross Point 50%, and Cross Point 30 to 80%@25 Gbit/s)	Tr/Tf, Total Jitter, Waveform
	Offset	-2.0 to +3.3 Voh, 1 mV Step (Independent, variable)	Distortion specified at
		Accuracy: ±65 mV ±10% of Offset(Vth) ± (Amplitude Accuracy/2)	point
		Current Limit (Sourcing 50 mA/Sinking 80 mA)	
	Defined Interface	NECL,SCFL,NCML,PCML,LVPECL,LVDS (400 mVp-p)	
	Cross Point	20 to 80%/0.1% Step (independent)	
	Tr/Tf	Typ.12 ps(20 to 80%)@25 Gbit/s, 1.75 Vp-p	
	Total Jitter	Typ. 8 psp-p* ²	
	Waveform Distortion (0-peak)	Typ. ±25 mV ±10%@25 Gbit/s Typ. ±25 mV ±15%@28 Gbit/s (when MU182020A-x01 installed) Typ. ±25 mV ±15%@28.1 Gbit/s (when MU182020A-x01+x03 installed)	
	ON •OFF	ON•OFF switchable	
	Termination	Can be switched between AC and DC,50 Ω GND,-2 V,+1.3 V,+3.3 V,Open(LVDS) (when DC selected)	
	Connector	K	
	Offset reference	Can be switched between Voh,Vth and Vol	
	Data/XData Tracking	Yes	
	Level Guard	Yes	
	External ATT Factor	Yes	

Table 1.3.1-1 Specifications for MU182020A (Cont'd)

*1: The specification of the data output waveforms is the value observed using application part J1439A, coaxial cable (0.8m, K connector) and sampling oscilloscope bandwidth of 70 GHz.

Item		Specifications	Remarks
Data Output*1 (continued)	Number of Output	2(Data/Data)	
MU182020A- x11	Amplitude	0.5 to $2.5~{\rm Vp}\mbox{-}{\rm p}\mbox{-}{\rm 2}$ mV Step (Independent, variable)	
(Variable Data Output (0.5 to 2.5 Vnrn))		Accuracy: $\pm 50 \text{ mV} \pm 17\%$ of Amplitude (Cross Point 50%, and Cross Point 30 to $80\%@25$ Gbit/s)	
2.5 vp-p//	Offset	-2.0 to +3.3 Voh, Min4.0 Vol/1 mV Step (Independent, variable)	
		Accuracy: ±65 mV ±10% of Offset(Vth) ± (Amplitude Accuracy/2)	
		Current Limit (Sourcing 50 mA/Sinking 80 mA)	
	Defined Interface	PCML,NCML,SCFL,NECL,LVPECL	
	Cross Point	20 to 80%/0.1% Step (independent)	
	Tr/Tf	Typ.12 ps (20 to 80%) @25 Gbit/s, 2.5 Vp-p	
	Total Jitter	Typ. 8 psp–p ^{*2}	
	Waveform Distortion (0-peak)	Typ. ±25 mV ±10%@25 Gbit/s Typ. ±25 mV ±15%@28 Gbit/s (when MU182020A-x01 installed) Typ. ±25 mV ±15%@28.1 Gbit/s (when MU182020A-x01+x03 installed)	
	ON•OFF	ON•OFF switchable	
	Termination	Can be switched between AC and DC,50 Ω GND,–2 V,+1.3 V (when DC selected)	
	Connector	К	
	Offset reference	Can be switched between Voh,Vth and Vol	
	Data/XData Tracking	Yes	
	Level Guard	Yes	
	External ATT Factor	Yes	

Table 1.3.1-1	Specifications	for MU182020A	(Cont'd)
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*1: The specification of the data output waveforms is the value observed using application part J1439A, coaxial cable (0.8m, K connector) and sampling oscilloscope bandwidth of 70 GHz.

1.3 Specifications

	ltem	Specifications	Remarks
Data Output*1	Number of Output	2 (Data/ Data)	
(continued) MU182020A-	Amplitude	0.5 to 3.5 Vp-p/2 mV Step (Independent, variable)	
x13 (Variable Data Output		Accuracy:±50 mV ±17% of Amplitude (Cross Point 50%, and Cross Point 30 to 80%@25 Gbit/s)	
(0.5 to 3.5 Vp-p))	Offset	-2.0 to +3.3 Voh, Min4.0 Vol/1 mV Step (Independent, variable)	
		Accuracy: ±65 mV ±10% of Offset(Vth) ± (Amplitude Accuracy/2) Current Limit (Sourcing 50 mA/Sinking 80	
		mA)	
	Defined Interface	PCML,NCML,SCFL,NECL,LVPECL	
	Cross Point	20 to 80%/0.1% Step (independent)	
	Tr/Tf	Typ.12 ps (20 to 80%)@25 Gbit/s, 3.5 Vp-p	
	Total Jitter	Typ. 8 psp ⁻ p ^{*2}	
	Waveform Distortion (0-peak)	Typ. ±25 mV ±10%@25 Gbit/s Typ. ±25 mV ±15%@28 Gbit/s (when MU182020A-x01 installed) Typ. ±25 mV ±15%@28.1 Gbit/s (when MU182020A-x01+x03 installed)	
	ON•OFF	ON•OFF switchable	
	Termination	Can be switched between AC and DC,50 Ω GND,–2 V,+1.3 V (when DC selected)	
	Connector	К	
	Offset reference	Can be switched between Voh,Vth and Vol	
	Data/XData Tracking	Yes	
	Level Guard	Yes	
	External ATT Factor	Yes	

Table 1.3.1-1 Specifications for MU182020A (Cont'd)

*1: The specification of the data output waveforms is the value observed using application part J1439A, coaxial cable (0.8m, K connector) and sampling oscilloscope bandwidth of 70 GHz.

	ltem	Specifications	Remarks
Clock Output*1	Number of Output	1	When MU182020A-x
	Amplitude	Min. 0.3 Vp-p, Max. 1.0 Vp-p Min. 0.7 Vp-p, Max. 1.0 Vp-p (When MU182020A-x02 is installed, and external clock input is 0.5 Vp-p or more)	21 is not installed* ²
	ON•OFF	ON•OFF switchable (When MU182020A-x02 is installed)	
	Termination	ΑC/50 Ω	
	Connector	SMA K(When MU182020A-x02 is installed)	
	Number of Output	1	When MU182020A-x
	Amplitude	0.5 to 2.0 Vp-p/2 mV Step (Independent, variable) Accuracy:±70 mV ±17% of Amplitude	21 is installed ^{*3}
	Offset	-2.0 to +3.3 Voh, Min4.0 Vol/1 mV Step (Independent, variable)	
		Accuracy: ±65 mV ±10% of Offset(Vth) ± (Amplitude Accuracy/2)	
		Current Limit (Sourcing 50 mA/Sinking 80 mA)	
	Defined Interface	PCML,NCML,SCFL,NECL,LVPECL	
	Duty Setting Range	-25 to +25/1 Step(No Unit)	
	ON •OFF	ON•OFF switchable	
	Termination	Can be switched between AC connection and DC connection, 50Ω GND, $-2 V$, $+1.3 V$ (when DC selected)	
	Connector	К	
	Offset reference	Can be switched between Voh,Vth and Vol	
	Level Guard	Yes	
	External ATT Factor	Yes	

Table 1.3.1-1 Specifications for MU182020A (Cont'd)

*1: The specification of the clock output waveforms is the value observed using sampling oscilloscope bandwidth of 50 GHz.

*2: The specification when MU182020A-x21 is not installed is the value observed using application part J1342A coaxial cable 0.8m (APC3.5 connector).

*3: The specification when MU182020A-x21 is not installed is the value observed using application part J1439A coaxial cable 0.8m (K connector).

Item		Specifications	Remarks
Variable Data Delay	Variable phase range	 -2000 to +2000 mUI/2 mUI Step (with MU181020A/B and installed in another mainframe and at Independent) -64000 to +64000 mUI/2 mUI Step (with MU181020A/B and installed in another mainframe and at 25G×2 Ch Combination/2 Ch Combination setting) 	When MU182020A -x30 or x31 is installed
	Phase setting error	Typ. ±50 mUIp-p	
	mUI-ps conversion	Available	
	Calibration	Available	
	Relative 0	Available	
Unit Sync	Unit Offset	-64000 to +64000 mUI, 2 mUI Step (Restrictions vary depending on the Delay setting values.)	Restrived depnding on Combinatio n Setting *
Dimension		234mm(W)×21mm(H)×175mm(D) (with Compact-PCI 1 slot but excluding protrusions)	
Mass		2.5 kg max. (including options)	
Environmental Performance	Operation Temperature	+15 to +35°C (ambient temperature around equipment when installed in the mainframe)	
	Storage Temperature	-20 to +60°C	

Table 1.3.1-1 Specifications for MU182020A (Cont'd)

*: This function is valid when it is set to 25Gx2ch Combination and Unit Sync. For more information about the Unit Sync, refer to the MU181020A/B Operation Manual.

1.3.2 Specifications for MU182021A

Table 1.3.2-1 Specifications for MU182021A

Item		Specifications	Remarks
Operating bit rate	9	8.0 to 25.0 Gbit/s 8.0 to 28.0 Gbit/s (When MU182021A-x01 is installed) 8.0 to 28.1 Gbit/s (When MU182021A-x01 ,x03 installed)	
External clock input	Number of Input	1	
	Frequency	4.0 to 12.5 GHz 4.0 to 14.0 GHz (When MU182021A-x01 is installed) 4.0 to 14.05 GHz (When MU182021A-x01, x03 installed)	
		4.0 to 12.5 GHz 8.0 to 25.0 GHz (switchable when MU182021A-x02 installed)	
		4.0 to 14.0 GHz 8.0 to 28.0 GHz (switchable when MU182021A-x01, x02 installed)	
		4.0 to 14.5 GHz 8.0 to 28.1 GHz (switchable when MU182021A-x01, x02, x03 installed)	
	Amplitude	0.3 to 1.0 Vp-p	
	Termination	ΑC/50 Ω	
	Connector	SMA (when MU182021A-x02 is not installed) K (when MU182021A-x02 installed)	
1/2 Data Input	Number of Input	4 (1/2Data Input 1A, 1/2 Data Input 1B, 1/2 Data Input 2A, 1/2 Data Input 2B)	From MU181020A/B Data Output
	Level	0/-1 V H:-0.25 to +0.05 V L:-1.4 to -0.85 V	
	Termination	50 Ω/GND	
	Connector	SMA	
1/2 Clock Input	Number of Input	1	From MU181020A/B
	Amplitude	0.25 to 1.0 Vp-p	Clock Output
	Termination	ΑC/50 Ω	
	Connector	SMA	

lte	m	Specifications	Remarks
1/2 Clock	Clock Output	4	То
Output	Amplitude	Min. 0.4 Vp-p, Max. 1.2 Vp-p	MU181020A/B
	Termination	ΑC/50 Ω	Ext Clock Input
	Connector	SMA	
	Between channels Skew	≤10 ps 12 GHz (when MU182021A-x01 uninstalled) 14 GHz (whenMU182021A-x01 installed) 14.05 GHz (whenMU182021A-x01+x03 installed)	

Table 1.3.2-1 Specifications for MU182021A (Cont'd)

Data Output MU182021A- x10 Number Output of Output 4(Data1/Data1,Data2/Data2) Defined with PRBS2 ³¹ (Variable Data Output (0.25 to 1.75 Vpp)) Amplitude 0.25 to 1.75 Vpp/2 mV Step (Independent, variable) Mark Ratio 1/2 Accuracy:±50 mV ±17% of Amplitude (Cross Point 50%, and Cross Point 30 to 80%@25 to 1.75 Vpp)) Tr/Tf, Total Jitter, Waveform Offset -2.0 to +3.3 Voh, 1 mV Step (Independent, variable) Tr/Tf, Total Jitter, Waveform Defined -2.0 to +3.3 Voh, 1 mV Step (Independent, variable) Waveform Distortion -2.0 to +3.3 Voh, 1 mV Step (Independent, variable) Waveform Distortion -2.0 to +3.3 Voh, 1 mV Step (Independent, variable) Waveform Defined NECL,SCFL,NCML,PCML,LVPECL,LVDS Interface Current Limit (Sourcing 50 mA/Sinking 80 mA) Defined NECL,SCFL,NCML,PCML,LVPECL,LVDS Interface 120 to 80%/0.1% Step (independent) Tr/Tf Typ.12 ps(20 to 80%)@25 Gbit/s Distortion Typ. ±25 mV ±15%@28 Gbit/s (0-peak) (when MU182021A-x01 installed) ON·OFF ON·OFF switchable Termination Can be switched between AC and DC,50 Q GND,-2 V, ±1.3 V, ±3.3 V,Open(LVDS) (when DC selected) Connector Current Limit Can be switched between Voh,Vth and Vol reference Data/XData Yes	Item		Specifications	Remarks
x10 (Variable Data Output (0.25 to 1.75 Vpp)) Amplitude 0.25 to 1.75 Vpp/2 mV Step (Independent, variable) Mark Ratio 1/2 Accuracy:±50 mV ±17% of Amplitude (Cross Point 50%, and Cross Point 30 to 80%@25 (Bit/s) Tr/Tf, Total Jitter, Waveform Offset -2.0 to +3.3 Voh, 1 mV Step (Independent, variable) Tr/Tf, Total Jitter, Waveform Offset -2.0 to +3.3 Voh, 1 mV Step (Independent, variable) Distortion specified at 50% Cross point Defined NECL,SCFL,NCML,PCML,LVPECL,LVDS Interface Current Limit (Sourcing 50 mA/Sinking 80 mA) Defined NECL,SCFL,NCML,PCML,LVPECL,LVDS Interface (400 mVpp) Corse Point 20 to 80%/0.1% Step (independent) Tr/Tf Typ.12 ps(20 to 80%)@25 Gbit/s, 1.75 Vpp Total Jitter Typ. ±25 mV ±15%@28 Gbit/s Distortion Typ. ±25 mV ±15%@28 Gbit/s ON+OFF ON+OFF switchable Termination Can be switched between AC and DC,50 Q (ND,-2 V,+1.3 V,+3.3 V,Open(LVDS) (when DC selected) Connector K Offset reference Can be switched between Voh,Vth and Vol reference Data/XData Tracking Yes Level Guard Yes	Data Output MU182021A-	Number of Output	4(Data1/Data1,Data2/Data2)	$\begin{array}{llllllllllllllllllllllllllllllllllll$
Output (0.25 to 1.75 Vp·p)) Accuracy:±50 mV ±17% of Amplitude (Cross Point 50%, and Cross Point 30 to 80%@25 Gbit/s) Jitter, Waveform Distortion specified at 50% Cross point Offset -2.0 to +3.3 Voh, 1 mV Step (Independent, variable) Mccuracy: ±65 mV ±10% of Offset(Vth) ± (Amplitude Accuracy/2) Waveform Distortion specified at 50% Cross point Defined NECL,SCFL,NCML,PCML,LVPECL,LVDS Interface Current Limit (Sourcing 50 mA/Sinking 80 mA) Defined NECL,SCFL,NCML,PCML,LVPECL,LVDS Interface (400 mVp·p) Cross Point 20 to 80%/0.1% Step (independent) Tr/Tf Typ. 12 ps(20 to 80%)@25 Gbit/s, 1.75 Vp·p Total Jitter Typ. ±25 mV ±10%@25 Gbit/s (0·peak) (when MU182021A-x01 installed) Typ. ±25 mV ±15%@28.1 Gbit/s (when MU182021A-x01 installed) ON·OFF ON·OFF switchable Termination Can be switched between AC and DC,50 Q GND,-2 V,+1.3 V,+3.3 V,Open(LVDS) (when DC selected) Connector K Offset reference Can be switched between Voh,Vth and Vol reference Data/XData Tracking Yes Level Guard Yes	x10 (Variable Data	Amplitude	0.25 to 1.75 Vp-p/2 mV Step (Independent, variable)	Mark Ratio 1/2
Offset $-2.0 \text{ to } +3.3 \text{ Voh, 1 mV Step (Independent, variable)}Distortion specified at 50% Cross pointAccuracy:±65 mV ±10% of Offset(Vth) ±(Amplitude Accuracy/2)Distortion specified at 50% Cross pointDefinedNECL,SCFL,NCML,PCML,LVPECL,LVDS(400 mVp-p)Cross Point20 to 80%/0.1% Step (independent)Tr/TfTyp. 12 ps(20 to 80%)@25 Gbit/s, 1.75 Vp-pTotal JitterTyp. 8 psp-*WaveformTyp. ±25 mV ±10%@25 Gbit/s(0'peak)(when MU182021A:x01 installed)(when MU182021A:x01 installed)ON·OFFON·OFF switchableTerminationCan be switched between AC and DC,50 Q(When DC selected)ConnectorKOffset(Can be switched between Voh,Vth and VolreferenceData/XDataTrackingYesLevel GuardYes$	Output (0.25 to 1.75 Vp-p))		Accuracy:±50 mV ±17% of Amplitude (Cross Point 50%, and Cross Point 30 to 80%@25 Gbit/s)	Tr/Tf, Total Jitter, Waveform
Accuracy: $\pm 65 \text{ mV} \pm 10\% \text{ of Offset(Vth)} \pm$ $(Amplitude Accuracy/2)$ $50\% \text{ Cross}$ pointCurrent Limit (Sourcing 50 mA/Sinking 80 mA)DefinedNECL,SCFL,NCML,PCML,LVPECL,LVDS (400 mVp·p)Cross Point20 to 80%/0.1% Step (independent)Tr/TfTyp.12 ps(20 to 80%)@25 Gbit/s, 1.75 Vp·pTotal JitterTyp. $\pm 25 \text{ mV} \pm 10\%@25 \text{ Gbit/s}$ (0-peak)(when MU182021A-x01 installed) Typ. $\pm 25 \text{ mV} \pm 15\%@28.1 \text{ Gbit/s}$ (when MU182021A-x01 installed)ON·OFFON·OFF switchableTerminationCan be switched between AC and DC,50 Ω (when DC selected)ConnectorKOffset referenceCan be switched between Voh,Vth and Vol referenceData/XData TrackingYesLevel GuardYesExtennelVac		Offset	-2.0 to +3.3 Voh, 1 mV Step (Independent, variable)	Distortion specified at
Current Limit Gourcing 50 mA/Sinking 80 mA)DefinedNECL,SCFL,NCML,PCML,LVPECL,LVDS InterfaceInterface(400 mVp·p)Cross Point20 to 80%/0.1% Step (independent)Tr/TfTyp.12 ps(20 to 80%)@25 Gbit/s, 1.75 Vp·pTotal JitterTyp. $\pm 25 \text{ mV} \pm 10\%@25 \text{ Gbit/s}$ DistortionTyp. $\pm 25 \text{ mV} \pm 15\%@28 \text{ Gbit/s}$ (0°peak)(when MU182021A*x01 installed) Typ. $\pm 25 \text{ mV} \pm 15\%@28.1 \text{ Gbit/s}$ (when MU182021A*x01+x03 installed)ON*OFFON*OFF switchableTerminationCan be switched between AC and DC,50 Q (when DC selected)ConnectorKOffset referenceCan be switched between Voh,Vth and Vol referenceData/XData TrackingYesLevel GuardYesExternalYes			Accuracy: ±65 mV ±10% of Offset(Vth) ± (Amplitude Accuracy/2)	50% Cross point
Defined InterfaceNECL,SCFL,NCML,PCML,LVPECL,LVDS (400 mVp·p)Cross Point20 to 80%/0.1% Step (independent)Tr/TfTyp.12 ps(20 to 80%)@25 Gbit/s, 1.75 Vp-pTotal JitterTyp. 8 psp·p*WaveformTyp. ±25 mV ±10%@25 Gbit/sDistortionTyp. ±25 mV ±15%@28 Gbit/s(0°peak)(when MU182021A-x01 installed)Typ. ±25 mV ±15%@28.1 Gbit/s(when MU182021A-x01+x03 installed)ON·OFFON·OFF switchableTerminationCan be switched between AC and DC,50 QGND,-2 V,+1.3 V,+3.3 V,Open(LVDS) (when DC selected)ConnectorKOffset referenceCan be switched between Voh,Vth and VolPata/XData TrackingYesLevel GuardYes			mA)	
$ \begin{array}{c c} Cross Point & 20 to 80\%/0.1\% Step (independent) \\ \hline Tr/Tf & Typ.12 ps(20 to 80\%)@25 Gbit/s, 1.75 Vp-p \\ \hline Total Jitter & Typ. 8 psp-p* \\ \hline Waveform & Typ. ±25 mV \pm 10\%@25 Gbit/s \\ Distortion & Typ. \pm 25 mV \pm 15\%@28 Gbit/s \\ (0-peak) & (when MU182021A-x01 installed) \\ Typ. \pm 25 mV \pm 15\%@28.1 Gbit/s \\ (when MU182021A-x01+x03 installed) \\ \hline ON \cdot OFF & ON \cdot OFF switchable \\ \hline Termination & Can be switched between AC and DC,50 \Omega \\ GND,-2 V,+1.3 V,+3.3 V,Open(LVDS) \\ (when DC selected) \\ \hline Connector & K \\ \hline Offset & Can be switched between Voh,Vth and Vol reference \\ \hline Data/XData & Yes \\ \hline Tracking & Level Guard & Yes \\ \hline \end{array} $		Defined Interface	NECL,SCFL,NCML,PCML,LVPECL,LVDS (400 mVp ⁻ p)	
$\begin{array}{c cccc} Tr/Tf & Typ.12 \ ps(20 \ to \ 80\%)@25 \ Gbit/s, 1.75 \ Vp\ p \\ \hline Total \ Jitter & Typ. 8 \ psp\ p^* \\ \hline Waveform & Typ. \pm 25 \ mV \pm 10\%@25 \ Gbit/s \\ Distortion & Typ. \pm 25 \ mV \pm 15\%@28 \ Gbit/s \\ (when \ MU182021A\ x01 \ installed) \\ Typ. \pm 25 \ mV \pm 15\%@28.1 \ Gbit/s \\ (when \ MU182021A\ x01\ x03 \ installed) \\ \hline ON \cdot OFF & ON \cdot OFF \ switchable \\ \hline Termination & Can be switched between \ AC \ and \ DC,50 \ \Omega \\ GND,-2 \ V,\pm1.3 \ V,\pm3.3 \ V,Open(LVDS) \\ (when \ DC \ selected) \\ \hline Connector & K \\ Offset & Can \ be \ switched \ between \ Voh, Vth \ and \ Vol \\ reference & \\ \hline Data/XData & Yes \\ \hline Tracking & \\ \hline Level \ Guard & Yes \\ \hline \end{array}$		Cross Point	20 to 80%/0.1% Step (independent)	
Total JitterTyp. 8 psp-p*WaveformTyp. $\pm 25 \text{ mV} \pm 10\%@25 \text{ Gbit/s}$ DistortionTyp. $\pm 25 \text{ mV} \pm 15\%@28 \text{ Gbit/s}$ (0-peak)(when MU182021A-x01 installed)Typ. $\pm 25 \text{ mV} \pm 15\%@28.1 \text{ Gbit/s}$ (when MU182021A-x01+x03 installed)ON·OFFON·OFF switchableTerminationCan be switched between AC and DC,50 Ω GND,-2 V,+1.3 V,+3.3 V,Open(LVDS)(when DC selected)ConnectorKOffsetCan be switched between Voh,Vth and VolreferenceData/XDataYesLevel GuardYes		Tr/Tf	Typ.12 ps(20 to 80%)@25 Gbit/s, 1.75 Vp-p	
WaveformTyp. $\pm 25 \text{ mV} \pm 10\%@25 \text{ Gbit/s}$ DistortionTyp. $\pm 25 \text{ mV} \pm 15\%@28 \text{ Gbit/s}$ (0-peak)(when MU182021A-x01 installed)Typ. $\pm 25 \text{ mV} \pm 15\%@28.1 \text{ Gbit/s}$ (when MU182021A-x01+x03 installed)ON•OFFON•OFF switchableTerminationCan be switched between AC and DC,50 Ω GND,-2 V,+1.3 V,+3.3 V,Open(LVDS)(when DC selected)ConnectorKOffsetCan be switched between Voh,Vth and VolreferenceData/XDataYesFurtermedYes		Total Jitter	Typ. 8 psp-p*	
ON·OFFON·OFF switchableTerminationCan be switched between AC and DC,50 Ω GND,-2 V,+1.3 V,+3.3 V,Open(LVDS) (when DC selected)ConnectorKOffset referenceCan be switched between Voh,Vth and Vol referenceData/XData TrackingYesLevel GuardYesFuternalYes		Waveform Distortion (0-peak)	Typ. ±25 mV ±10%@25 Gbit/s Typ. ±25 mV ±15%@28 Gbit/s (when MU182021A-x01 installed) Typ. ±25 mV ±15%@28.1 Gbit/s (when MU182021A-x01+x03 installed)	
TerminationCan be switched between AC and DC,50 Ω GND,-2 V,+1.3 V,+3.3 V,Open(LVDS) (when DC selected)ConnectorKOffset referenceCan be switched between Voh,Vth and Vol referenceData/XData TrackingYesLevel GuardYesFuternalYes		ON •OFF	ON•OFF switchable	
ConnectorKOffset referenceCan be switched between Voh,Vth and VolData/XData TrackingYesLevel GuardYesFuternalYes		Termination	Can be switched between AC and DC,50 Ω GND,-2 V,+1.3 V,+3.3 V,Open(LVDS) (when DC selected)	
Offset referenceCan be switched between Voh,Vth and VolData/XData TrackingYesLevel GuardYesFuternalYes		Connector	К	
Data/XData TrackingYesLevel GuardYesFuternalYes		Offset reference	Can be switched between Voh,Vth and Vol	
Level Guard Yes		Data/XData Tracking	Yes	
Futomol Voc		Level Guard	Yes	
ATT Factor		External ATT Factor	Yes	

Table 1.3.2-1	Specifications for MU182021A	(Cont'd)

lt	em	Specifications	Remarks
Data Output*1 (continued)	Number of Output	$4(Data1/\overline{Data1}, Data2/\overline{Data2})$	
MU182021A- x11	Amplitude	0.5 to 2.5 Vp-p/2 mV Step (Independent, variable)	
(Variable Data Output (0.5 to		Accuracy:±50 mV ±17% of Amplitude (Cross Point 50%, and Cross Point 30 to 80%@25 Gbit/s)	
2.5 v p-p//	Offset	-2.0 to +3.3 Voh, Min4.0 Vol/1 mV Step (Independent, variable)	
		Accuracy: ±65 mV ±10% of Offset(Vth) ± (Amplitude Accuracy/2)	
		Current Limit (Sourcing 50 mA/Sinking 80 mA)	
	Defined Interface	PCML,NCML,SCFL,NECL,LVPECL	
	Cross Point	20 to 80%/0.1% Step (independent)	
	Tr/Tf	Typ.12 ps(20 to 80%)@25 Gbit/s, 2.5 Vp-p	
	Total Jitter	Typ. 8 psp-p* ²	
	Waveform Distortion (0-peak)	Typ. ±25 mV ±10%@25 Gbit/s Typ. ±25 mV ±15%@28 Gbit/s (when MU182021A-x01 installed) Typ. ±25 mV ±15%@28.1 Gbit/s (when MU182021A-x01+x03 installed)	
	ON •OFF	ON•OFF switchable	
	Data1/Data2 Skew	±0.25 UI (Refer to MU182021A-x10 Data1/Data2 Skew.)	
	Termination	Can be switched between AC and DC,50 Ω GND,–2 V,+1.3 V(when DC selected)	
	Connector	К	
	Offset reference	Can be switched between Voh,Vth and Vol	
	Data/XData Tracking	Yes	
	Level Guard	Yes	
	External ATT Factor	Yes	

Table 1.3.2-1 Specifications for MU182021A (Cont'd)

*1: The specification of the data output waveforms is the value observed using application part J1439A, coaxial cable (0.8m, K connector) and sampling oscilloscope bandwidth of 70 GHz.

	Item	Specifications	Remarks
Data Output*1	Number of Output	$4(Data1/\overline{Data1}, Data2/\overline{Data2})$	
(continued) MU182021A-	Amplitude	0.5 to 3.5 Vp-p/2 mV Step (Independent, variable)	
x13 (Variable Data Output		Accuracy:±50 mV ±17% of Amplitude (Cross Point 50%, and Cross Point 30 to 80%@25 Gbit/s)	
(0.5 to 3.5 Vp-p))	Offset	-2.0 to +3.3 Voh, Min4.0 Vol/1 mV Step (Independent, variable)	
		Accuracy: ±65 mV ±10% of Offset(Vth) ± (Amplitude Accuracy/2)	
		Current Limit (Sourcing 50 mA/Sinking 80 mA)	
	Defined Interface	PCML,NCML,SCFL,NECL,LVPECL	
	Cross Point	20 to 80%/0.1% Step (independent)	
	Tr/Tf	Typ.12 ps (20 to 80%)@25 Gbit/s, 3.5 Vp-p	
	Total Jitter	Тур. 8 psp-p*2	
	Waveform Distortion (0-peak)	Typ. ±25 mV ±10%@25 Gbit/s Typ. ±25 mV ±15%@28 Gbit/s (when MU182021A-x01 installed) Typ. ±25 mV ±15%@28.1 Gbit/s (when MU182020A-x01+x03 installed)	
	ON •OFF	ON•OFF switchable	
	Data1/Data2 Skew	±0.25 UI (Refer to MU182021A-x10 Data1/Data2 Skew.)	
	Termination	Can be switched between AC and DC,50 Ω GND,–2 V,+1.3 V(when DC selected)	
	Connector	К	
	Offset reference	Can be switched between Voh,Vth and Vol	
	Data/XData Tracking	Yes	
	Level Guard	Yes	
	External ATT Factor	Yes	

Table 1.3.2-1 Specifications for MU182021A (Cont'd)

*1: The specification of the data output waveforms is the value observed using application part J1439A, coaxial cable (0.8m, K connector) and sampling oscilloscope bandwidth of 70 GHz.

	ltem	Specifications	Remarks
Clock Output*1	Number of Output	1	When MU182021A-x
	Amplitude	Min. 0.3 Vp-p, Max. 1.0 Vp-p Min. 0.7 Vp-p, Max. 1.0 Vp-p (When MU182021A-x02 is installed, and external clock input is 0.5 Vp-p or more)	21 is not installed* ²
	ON•OFF	ON•OFF switchable (When MU182021A-x02 is installed)	
	Termination	ΑC/50 Ω	
	Connector	SMA K(When MU182021A-x02 is installed)	
	Number of Output	$2(\text{Clock}, \overline{\text{Clock}})$	When MU182021A-x
	Amplitude	0.5 to 2.0 Vp-p/2 mV Step Accuracy:±70 mV ±17% of Amplitude	21 is installed ^{*3}
	Offset	-2.0 to +3.3 Voh, Min4.0 Vol/1 mV Step (Independent, variable)	
		Accuracy: ±65 mV ±10% of Offset(Vth) ± (Amplitude Accuracy/2)	
		Current Limit (Sourcing 50 mA/Sinking 80 mA)	
	Defined Interface	PCML,NCML,SCFL,NECL,LVPECL	
	Duty Setting Range	-25 to +25/1 Step (No Unit, Clock/XClock Not independent)	
	ON •OFF	ON•OFF switchable	
	Termination	Can be switched between AC connection and DC connection, 50Ω GND, $-2 V$, $+1.3 V$ (when DC selected)	
	Connector	К	
	Offset reference	Can be switched between Voh,Vth and Vol	
	Tracking	Yes	
	Level Guard	Yes	
	External ATT Factor	Yes	

Table 1.3.2-1 Specifications for MU182021A (Cont'd)

*1: The specification of the clock output waveforms is the value observed using sampling oscilloscope bandwidth of 50 GHz.

- *2: The specification when MU182021A-x21 is not installed is the value observed using application part J1342A coaxial cable 0.8m (APC3.5 connector).
- *3: The specification when MU182021A-x21 is not installed is the value observed using application part J1439A coaxial cable 0.8m (K connector).

lt	em	Specifications	Remarks
Variable Data Delay	Variable phase range	 -2000 to +2000 mUI/2 mUI Step (When installed in a different unit from MU181020A/B, or when being Independent -64000 to +64000 mUI/2 mUI Step (When installed in the same unit with MU181020A/B and in 25G × 2ch Combination/2ch Combination/25G CH Sync) 	When MU182021A -x30 or x31 is installed
	Phase setting error	Typ. ±50 mUIp-p	
	mUI-ps conversion	Available	
	Calibration	Available	
	Relative 0	Available	
Emphasis Control	Emphasis Output ON•OFF	ON•OFF switchable	When MU182021A -x40 is
	Data/XData Tracking	Yes	installed
	Defined Interface	Variable	
	Amplitude	Setting range varies with MUX output option, Emphasis Amplitude Ratio, and external ATT. The default setting range for Emphasis Amplitude Ratio, EXT ATT Factor, and offset is shown below. MU182021A-010:0.132 to 0.856 V MU182021A-011:0.262 to 1.224 V MU182021A-013:0.262 to 1.714 V The default is 0.6 Vp-p.	
	Emphasis Amplitude Ratio	Setting range varies with MUX output option, output amplitude and external ATT -9.0 to +9.0 dB/0.1 dB Step Initial setting value:-9 dB -/+ switchable	
	EXT ATT Factor (Data1)	0 to 40 dB Initial setting value:3 dB	
	EXT ATT Factor (Data2)	0 to 40 dB Initial setting value:10 dB	
	Offset	Settable range depends on MUXs output option, output amplitude, Emphasis Amplitude Ratio,and external ATT. Initial setting value:0 V(Vth) (Independent, variable) AC ON•OFF switchable	
	Emphasis Pulse Width	-500 to +1500 mUI/2 mUI steps With mUI-ps conversion	

Table 1.3.2-1 Specifications for MU182021A (Cont'd)

ltem		Specifications	Remarks
Emphasis Control (Cont'd)	Delay	-2000 to +2000 mUI/2 mUI steps With mUI-ps conversion With Calibration	
Pattern	${ m Data1} imes 2 \ { m Combination} \ (25{ m G} \ { m x} 2{ m ch} \ { m Combination})$	Data occurrence order Data 1A 1,5,9,13,17, Data 1B 3,7,11,15,19, Data 2A 2,6,10,14,18, Data 2B 4,8,12,16,20,	Function as 25Gbit/s PPG
	Data1/2 Combination (2ch Combination)	Data occurrence order Data 1A 1,3,5,7,9, Data 1B 2,4,6,8,10, Data 2A 1',3',5',7',9', Data 2B 2',4',6',8',10',	
	Data1/2 Synchronization (25G CH Sync)	Data occurrence order Data 1A 1,3,5,7,9, Data 1B 2,4,6,8,10, Data 2A 1',3',5',7',9', Data 2B 2',4',6',8',10',	
Unit Sync	Unit Offset	-64000 to +64000 mUI, 2 mUI Step (Restrictions vary depending on the Delay setting values.)	Restrived depnding on Combinatio n Setting *
Dimension		234mm(W)×21mm(H)×175mm(D) (with Compact-PCI 1 slot but excluding protrusions)	
Mass	_	5.0 kg max. (including options)	
Environmental Performance	Operation Temperature	+15 to +35°C (ambient temperature around equipment when installed in the main unit)	
	Storage Temperature	-20 to +60°C	

Table 1.3.2-1 Specifications for MU182021A (Cont'd)

This function is valid when it is set to 25Gx2ch Combination or 25G Channel Synchronization and Unit Sync. For more information about the Unit Sync, refer to the MU181020A/B Operation Manual.

Note:

*:

The MU182021A-x40 Emphasis settings screen is enabled when the Combination Setting status is 25G CH Synchronization.
Chapter 2 Preparation before Use

This chapter describes preparations required before using the MU182020A/21A.

2.1	Installation to Signal Quality Analyzer	2-2
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2.1 Installation to Signal Quality Analyzer

For information on how to install the MU182020A/21A to the Signal Quality Analyzer and how to turn on the power, refer to Chapter 2 "Preparation before Use" in the Signal Quality Analyzer Series Installation Guide.

For the installation position of the mainframe, refer to the release note included in this equipment or refer to the Anritsu homepage (<u>http://www.anritsu.com</u>).

2.2 How to Operate Application

The modules connected to the Signal Quality Analyzer are controlled by operating the MX180000A Signal Quality Analyzer Control Software (hereinafter, referred to as "MX180000A").

For information on how to start up, shut down, and operate the MX180000A, refer to the MX180000A Signal Quality Analyzer Control Software Operation Manual.

2.3 Preventing Damage

Be sure to observe the rating ranges when connecting input and output of the MU182020A/21A. Otherwise, the MU182020A/21A may be damaged.

CAUTION A

- 1. When signals are input to the MU182020A/21A, avoid excessive voltage beyond the rating. Otherwise, the circuit may be damaged.
- 2. When output is used at the 50 Ω /GND terminator, never feed any current or input signals to the output.
- 3. As a countermeasure against static electricity, ground other devices to be connected (including experimental circuits) with ground wires before connecting the I/O connector.
- 4. The outer conductor and core of the coaxial cable may become charged as a capacitor. Use any metal to discharge the outer conductor and core before use.
- 5. Never open the MU182020A/21A. If you open it and MU182020A/21A has failed or sufficient performance cannot be obtained, we may decline to repair the MU182020A/21A.
- The MU182020A/21A incorporates important parts and circuits, such as a hybrid IC, which are vulnerable to static electricity. Do not open the MU182020A/21A to touch such components.
- The hybrid IC incorporated in the MU182020A/21A is hermetically shielded. Do not open the hybrid IC. If you open it and sufficient performance cannot be obtained, we may decline to repair the MU182020A/21A.

- 8. To protect the MU182020A/21A from electrostatic discharge failure, a conductive sheet should be placed onto the workbench, and the operator should wear an electrostatic discharge wrist strap. Connect the ground connection end of the wrist strap to the conductive sheet or to the ground terminal of the mainframe.
- 9. When connecting an external device such as a Bias-T to the output connectors of this equipment (PPG or MUX), if the output signal includes any DC voltage, variations in the output of the DC power supply or load may change the level of the output signal, risking damage to the internal circuits. Note the following precautions when using this equipment:

1. Do not connect or disconnect any external devices while DC voltage is impressed.

2. Only switch DC power sources ON and OFF when all equipment connections have been completed.

<Recommended procedure>

Measurement Preparation 1:

- 1. Connect all equipment.
- 2. Set the DC power supply output to ON.

3. Set the equipment output to ON and complete measurement.

Measurement Preparation 2:

- 1. Set the equipment output to OFF.
- 2. Set the DC power supply output to OFF.

3. Disconnect the equipment, or change the DUT connections.

Since even unforeseen fluctuations in DC voltage and load (open or short circuits at the equipment output side and changes caused by using a high-frequency probe, etc.,) can damage the DUT and equipment, we recommend connecting a 50–ohm resistance in series with the DC terminal of the Bias-T to prevent risk of damage.

2.3 Preventing Damage



Do not connect/disconnect while DC voltage impressed.



Chapter 3 Panel Layout and Connectors

This chapter describes the panel and connectors of the MU182020A/21A.

3.1	Panel	Layout	3-2
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	3.1.2	MU182021A Panel	3-3
3.2	Inter-N	Iodule Connection	3-4

3.1 Panel Layout

3.1.1 MU182020A Panel



Table 3.1.1-1	Connectors on MU182020A panel
---------------	-------------------------------

No.	Name	Description		
[1]	1/2 Data Input A connectors	Inputs for data signals from dual MU181020A/B		
	1/2 Data Input B connectors	Multiplexes signal to Data Output		
[2]	1/2 Clock Input connector	Inputs for Clock signal from MU181020A/B		
[3]	Data Output connectors Output for 2:1 multiplexed differential data signal			
XData Output connectors Suppor		Supports various interfaces by selecting option		
[4]	Clock Output connector	Output for Clock signal		
		Same output frequency as Clock input to Ext. Clock Input		
[5]	1/2 Clock Output connector	Output for dual MU181020A/B reference Clock		
[6]	Ext. Clock Input connector	Inputs the clock signal output from the MU181000A 12.5 GHz		
		Synthesizer (hereinafter, referred to as "MU181000A") and		
		MG3693B synthesized signal generator (hereinafter, referred to as "MG3693B").		

3.1.2 MU182021A Panel



Table 3.1.2-1 Connectors on MU182021A panel

No.	Name	Description		
[1]	1/2 Data Input 1A connectors 1/2 Data Input 1B connectors	Inputs for data signals from dual MU181020A/B Multiplexes signal to Data Output1		
[2]	1/2 Data Input 2A connectors 1/2 Data Input 2B connectors	Inputs for data signals from dual MU181020A/B Multiplexes signal to Data Output2		
[3]	1/2 Clock Input connector	Inputs for Clock signal from MU181020A/B		
[4]	Data Output1 connectors XData Output1 connectors	Output for 2:1 multiplexed differential data signal Multiplexed output of 1/2 Data Input 1A and 1B signals		
[5]	Data Output2 connectors XData Output2 connectors	Output for 2:1 multiplexed differential data signal Multiplexed output of 1/2 Data Input 2A and 2B signals		
[6]	Clock Output connector XClock Output connector	Output for differential Clock signal Same output frequency as Clock input to Ext. Clock Input		
[7]	1/2 Clock Output connector	Output for fourfold MU181020A/B reference Clock		
[8]	Ext. Clock Input connector	Inputs the clock signal output from the MU181000A and MG3693B.		

3.2 Inter-Module Connection

A connection example between the MU182020/21A and MU181020B 14 Gbit/s PPG (hereinafter, referred to as "MU181020B") that are installed into a mainframe is shown below. Use the following procedure to connect these devices, and refer to Fig. 3.2-1 and Fig. 3.2-2.

Note:

Avoid static electricity when handling the devices.



Fig. 3.2-1 Inter-module connection example for MU182020A

- Use coaxial cables to connect the Ext. Clock Input connectors of the two MU181020B units with the 1/2 Clock Output connectors of this module. Ensure that the coaxial cables are exactly the same length or use the supplied accessory cables (J1427A or J1448A).
- 2. Use coaxial cables to connect the Data Output connectors of the two MU181020B units with the 1/2 Data Input A,B connectors of this module. Ensure that the coaxial cables are exactly the same length or use the supplied accessory cables (J1427A or J1448A).
- 3. Use coaxial cables to connect the Clock Output connectors of the MU181020B units with the 1/2 Clock Input connectors of this module. For the coaxial cables in Figure 3.2-1, the supplied accessory cables (J1427A or J1448A) are used.
- 4. Use a coaxial cable to connect the Clock signal source with the Ext. Clock Input connector of this module.

3.2 Inter-Module Connection



Fig. 3.2-2 Inter-module connection example for MU182021A

- 1. Use coaxial cables to connect the Ext. Clock Input connectors of the four MU181020B units with the 1/2 Clock Output connectors of this module. Ensure that the coaxial cables are exactly the same length or use the supplied accessory cables (J1428A).
- 2. Use coaxial cables to connect the Data Output connectors of the four MU181020B units with the 1/2 Data Input 1A, 1B, 2A, 2B connectors of this module. Ensure that the coaxial cables are exactly the same length or use the supplied accessory cables (J1428A).
- 3. Use a coaxial cable to connect the Clock Output connector of the MU181020B with the 1/2 Clock Input connector of this module.
- 4. Use a coaxial cable to connect the Clock signal source with the Ext. Clock Input connector of this module.



- 1. When signals are input to this MU182020A/21A, avoid excessive voltage beyond the rating. Otherwise, the circuit may be damaged.
- 2. As a countermeasure against static electricity, ground other devices to be connected (including experimental circuits) with ground wires before connecting the I/O connector.
- 3. The outer conductor and core of the coaxial cable may become charged as a capacitor. Use any metal to discharge the outer conductor and core before use.

- 4. The power supply voltage rating for the mainframe is shown on the rear panel. Be sure to operate the mainframe within the rated voltage range. The mainframe may be damaged if a voltage out of the rating range is applied.
- 5. To protect the MU182020A/21A from electrostatic discharge failure, a conductive sheet should be placed onto the workbench, and the operator should wear an electrostatic discharge wrist strap. Connect the ground connection end of the wrist strap to the conductive sheet or to the ground terminal of the mainframe.
- 6. When removing a cable from a connector on the front panel of the MU182020A/21A, be careful not to add excessive stress to the connector. Addition of excessive stress to a connector may result in characteristic degradation or a failure. Use a torque wrench (recommended torque: 0.9 N-M) when attaching or removing a cable.

Chapter 4 Configuration of Setup Dialog Box

This chapter explains the functions of each tab in the module procedure window.

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4.1 Configuration of Entire Setup Dialog Box

The configuration of the setup dialog box when the MU182020A/21A is inserted into a mainframe is shown below.



Fig. 4.1-1 Configuration of entire setup dialog box

The setup dialog box mainly consists of four blocks ([1] to [4] in the figure above). The following table describes each of the blocks.

No.	Block	Function		
[1]	Menu bar	Selects the setting functions related to the entire device.		
[2]	Module function buttons	Shortcut buttons for the function items specific to the displayed module. Users can customize up to 17 pre-defined function buttons according to their own applications.		
[3]	Function setting selection tabs	Click to switch the module operation tab window according to the function items.		
[4]	Operation tab window	Configures settings specific to each module.		

Table 4.1-1 Functions of blocks

4.2 Operation Tab Windows

The MU182020A/21A operation tab windows are listed below.

1:6:1] 25Gbit/s 2ch MUX				
Data1 Interface	Data2 Interface	Clock Interface		

Fig. 4.2-1 Function setting selection tabs

Tab name	Functions		
Data1 Interface	Selection and setting of Data1/XData1		
	Various output interface settings can be configured in this tab window.		
Data2 Interface	Selection and setting of Data2/XData2		
	Various output interface settings can be configured in this tab window.		
	This displays when the only MU182021A is installed.		
Clock Interface	Selection and setting of Clock/XClock		
	Various output interface settings can be configured in this tab window.		
	This displays when MU182020A-x02/x21 or MU182021A-x02/x21 is installed.		

Table 4.2-1 Function setting selection tabs

4.3 Setting Output Interface

To set the output interface, select the Data1 Interface and Data2 Interface tabs of the Operation screen

The screen Data and $\overline{\text{Data}}$ settings each correspond to the signals output from the Data and $\overline{\text{Data}}$ connectors, respectively. The following explains the settings related to the $\overline{\text{Data}}$ connector called XData.

4.3.1 Setting Data/XData





[1] Select ON or OFF for the data output.

When turning ON the Output signal, set the Output of the signal generator to ON, and in addition to this configuration, set the Output of the entire equipment to ON by the Module function button on the menu bar. [2] Select the offset reference. The Offset and Amplitude settings are restricted according to the set offset reference and the currently set Offset and Amplitude. In addition, when changing the offset reference, the offset value is also changed according to the set reference.

Offset reference Description		
Voh	The offset value is set based on the high level.	
Vth	The offset value is set based on the center level between the high and low levels.	
Vol	The offset value is set based on the low level.	

Table 4.3.1-1 Offset reference



Fig. 4.3.1-2 Setting data offset

- [3] The bit rate of the output data signal is displayed.
- [4] When Data1/Data2 Tracking is ON, the settings for Defined Interface, Amplitude, Offset, External ATT Factor, and Cross Point of Data 2 become the same as the Data1 settings. (The MU182020A does not support this function.)
- [5] When Tracking is set to ON, the settings for the XData become the same as those for the Data.
- [6] Click [Setup] to open the setup dialog box, and set the maximum amplitude (Amplitude), maximum offset (Offset Max (Voh); maximum value of the offset high level), and minimum offset (Offset Min (Vol); minimum value of the offset low level) for level guard. When Level Guard is set to ON, the Amplitude and Offset are restricted to the range set at [Setup] to ensure that the above required voltage is not applied to the DUT.

When the external ATT factor is set (see [8] below), the level guard settings (Amplitude, Offset Max (Voh), and Offset Min (Vol)) after passing through the fixed attenuator, which is connected between the MU181020A and the DUT, limit the output level of these setting value. Therefore, if you use the fixed attenuator without connecting, a signal exceeding the setting value is output. [7] Separately configure the defined interface setting for Data and XData.

Sometimes, some items cannot be selected, depending on the installed data output options and the Level Guard setting.

ltom	Amplitude		Offset	
item	Voh	Vol	Vth	
Variable	_	_	_	
PCML	+3.3 V	+2.8 V	+3.05 V	
NCML	0.0 V	$-0.5 \mathrm{V}$	$-0.25~\mathrm{V}$	
SCFL	0.0 V	–0.9 V	$-0.45~\mathrm{V}$	
NECL	-0.9 V	$-1.7 \mathrm{V}$	-1.3 V	
LVPECL	+2.4 V	+1.6 V	+2.0 V	
LVDS (400 mV)	+1.4 V	+1.0 V	+1.2 V	

Table 4.3.1-2 Amplitude setting values

[8] Separately set the amplitude for Data and XData.

The setting range varies depending on the level guard setting, offset setting, and installed option.

The amplitude setting ranges when Defined Interface is set to Variable are shown in the table below.

Table 4.3.1-3 Amplitude setting range

Installed Option Amplitude setting range		Resolution
x10	0.25 to 1.75 Vp-p	0.002 V
x11	0.5 to 2.5 Vp-p	0.002 V
x13	0.5 to 3.5 Vp-p	0.002 V

[9] Separately set the offset for Data and XData.

The setting range varies depending on the level guard setting, amplitude setting, and installed option.

The offset setting ranges when Defined Interface is set to Variable are shown in the table below.

Clicking to change [AC OFF] to [AC ON] enables AC-coupled output. The lowerband cutoff frequency is about 100 kHz.

Installed Option	Offset setting range	Resolution
x10	-3.75 to $3.3~\mathrm{V}$	0.001 V
x11	-4.0 to 3.3 V	0.001 V
x13	-4.0 to 3.3 V	0.001 V

Table 4.3.1-4 Offset setting range

- [10] Separately set the external ATT factor for Data and XData. When a fixed attenuator is connected to the Data/XData output connector of the MU181020A, the attenuation of the attenuator is added to the value for the DUT and displayed. A value from 0 to 40 dB can be set in 1-dB steps. When Defined Interface is not set to Variable, the setting is reset to 0 and becomes invalid. Values displayed in the External ATT Factor-Amplitude and Offset display areas indicate the amplitude and offset value after passing through the attenuator, respectively.
- [11] Separately set the cross point setting for Data and XData.

Table 4.3.1-5 Cross point setting range

Installed Option Cross point setting range		Resolution	
x10,x11,x13	20.0 to $80.0%$	0.1%	

[12] Set the Half Period Jitter for the data output signal. The Cross Point time axis can be adjusted as shown in Figure 4.3.1-3 using this setting while observing the Eye pattern.

Table 4.3.1-6 Half Period Jitter setting range

Setting values	Resolution
-20 to 20	1
20 to 20	1



Fig. 4.3.1-3 Setting Half Period Jitter

Notes:

- 1. The DUT may be damaged if the output setting is configured incorrectly. To prevent damage to the DUT, confirming the interface condition with the DUT, or configuring the level guard setting before making the output setting is recommended.
- 2. When PCML, LVPECL, or ECL is selected for Defined Interface, the voltage corresponding to the DUT's termination voltage is applied to the output side of the MU182020A. In this event, the DUT may be damaged if the interface conditions do not match. Be sure to confirm the interface conditions.
- 3. Waveforms may be distorted (what is known as a ringing phenomenon) when a commercially available ECL terminator is used to observe output waveforms. This is, however, caused by the characteristics of the ECL terminator; the waveform output from the mainframe is not distorted.
- 4. The current for the output part is limited (50 mA for sourcing current and 80 mA for sinking current) for protection. Sometimes, the observed waveform offset voltage may not match the set offset voltage when, for example, connected under the wrong interface conditions.
- 5. Be sure to confirm that a fixed attenuator is connected between the MU182020A and the DUT before setting the external ATT factor. If the external ATT factor is set when no fixed attenuator is connected or when the fixed attenuator has an attenuation value less than that set in the External ATT Factor area, the DUT may be damaged.

4.3.2 Setting delay

When MU182020A-x30 is installed into the MU182020A, the phase of the data output can be changed relative to the clock output.







Fig. 4.3.2-2 Output tab window for setting delay

[1] Click [Calibration] to perform calibration, which is a phase variable function. When the power is supplied, the frequency is changed, or the ambient temperature fluctuates, the calibration prompting alarm LED lights up. In such a case, click this button to perform calibration. When the LED indicator on the button is red, it is recommended to perform calibration. When the LED indicator is green, it shows the unit is well calibrated.

As the delay amount varies significantly during execution of calibration, keep this in mind for execution during measurement. Calibration will finish within 1 second.

[2] Set the delay in mUI or ps units.

<In the case of mUI units>

When this module and the MU181020A/B are both installed at the same time in the mainframe, and 2 Ch Combination, $25G \times 2$ Ch Combination or 25G Channel Synchronization are set, setting is supported from -64,000 to 64,000 mUI in 1-mUI steps.

At other than above: -2,000 to 2,000 mUI

<In the case of ps units>

The delay can be set in steps of ps units, equivalent to 2 mUI. The setting range is the range converting -64000 to 64000 mUI (-2000 to 2000 mUI) in ps units.

Example:

25 GHz: -2560 to 2560 ps, 0.08 ps steps

12.5 GHz: -5120 to 5120 ps, 0.16 ps steps

When the red frequency counter value range is incorrect, $\lceil ---- ps \rfloor$ is displayed.

Note:

When MU181020A/B and this equipment are mounted in the same unit with 2ch Combination or 25Gx2ch Combination selected, the delay settings of MU181020A/B and this equipment are interlinked. For the setting varies in conjunction with this module and the MU181020A/B, refer to Appendix B.4 Combination Operation.

- [3] Click [Relative] to use the current set phase value as the reference of relative 0 for delay setting.
 Pressing [Relative] allows you to set the current delay amount in units of "2 mUI" relative to the reference. When the [Relative] button is pressed again, the setting is converted from the relative value to the current delay value.
- [4] Set the jitter input.

ON: Select when inputting Jitter clock to this module. OFF: Default setting

[5] Set the Delay offset per the main frame.

This is valid only when the Unit Sync is set to On. And then, the common value is set in all MU182020A/21A installed in the same main frame.

This can be set per 2 mUI step within the range from -64,000 to 64,000 mUI.

However, the setting range is restricted depending on the Delay setting value at [2]. So, the setting range is : Delay setting value + Unit Offset setting value=+/-64000mUI

Notes:

- 1. When the frequency or the temperature condition is changed, the LED on the [Calibration] lights, prompting performance of calibration. If calibration is not performed at this time, the error in the phase setting may be greater than at a normal phase setting.
- 2. Values displayed in ps units vary as the frequency changes, because the MU181020A sets phases in mUI units as an internal standard.
- 3. When Burst is selected at Pattern Sequence of the Misc screen, the phase setting accuracy becomes worse than when Repeat is selected.
- 4. When inputting a jitter-modulated clock while Jitter Input of Delay is OFF, sometimes, the phase becomes unstable.
- 5. When inputting a jitter-modulated clock, if the Delay lamp is lit, sometimes, the phase setting error becomes large.
- 6. When inputting a signal to this module, do not input a voltage exceeding the specified value, otherwise the circuits may be damaged.
- 7. As countermeasure to static electricity, before connecting to an input connector, always ground the other equipment (including test circuit).
- 8. Sometimes, a coaxial cable can accumulate a charge between the outer and inner conductors rather like a capacitor. Always take antistatic measures such as grounding the outer conductor before connecting the cable.

Adjusting MU182021A 2 Ch data skew

When using the MU182021A, the data skew between two data signals can be adjusted using the delay setting.



Fig. 4.3.2-3 Delay setting in the case of Combination

4.3.3 Setting clock

Using this module, the clock output can be set when the MU182020A-x02/x21 or MU182021A-x02/x21 is installed.

Data1 Interface	Data2 Interface	Clock Interfac	e]	
Output				
Clock/XClock	ON 💌	Offset <mark>∨th</mark>	•	
Tracking	OFF			
Level Guard	OFF Set	up		
Define dilateri	Clock		XClock	_
	ace Varia		Variable	•
Amplitude	e 1.00	0 🕂 ∨pp	1.000	Vpp
				V
External A	IT Factor			d₿
– Amplit	ude	1.000 Vpp	1.000	Vpp
LOffse	: <u> </u>	0.000 V	0.000	V
Duty	0	<u>+</u>		
-Input	_		_	
Clock Input Ba	nd Switch Half	Rate Clock	•	
<u> </u>				

Fig. 4.3.3-1 Output tab window for setting clock

- Select ON or OFF for the clock output. The following explains Clock/XClock but since there is no XClock output when using the MU182020A, there are no panel displays or settings related to XClock.
- [2] Select the offset reference. The Offset and Amplitude settings are restricted according to the set offset reference and the currently set Offset and Amplitude. In addition, when changing the offset reference, the offset value is also changed according to the set reference.

Chapter 4 Configuration of Setup Dialog Box

Offset reference	Description		
Voh	The offset value is set based on the high level.		
Vth	The offset value is set based on the center level between the high and low levels.		
Vol	The offset value is set based on the low level.		

Table 4.3.3-1 Offset reference



Fig. 4.3.3-2 Setting clock offset

- [3] Set Tracking ON/OFF. When Tracking is set to ON, the settings for the XClock become the same as those for the Clock. (The MU182020A does not have this function.)
- [4] Configure the level guard setting. Click [Setup] to open the setup dialog box, and set the maximum amplitude, maximum offset (maximum value of the offset high level), and minimum offset (minimum value of the offset low level) for level guard, so that an excessively high voltage is not applied to the DUT.

When the external ATT factor is set (see [8] below), the level guard settings (Amplitude, Offset Max (Voh), and Offset Min (Vol)) after passing through the fixed attenuator, which is connected between the MU182020A and the DUT, limit the output level of these setting value. Therefore, if you use the fixed attenuator without connecting, a signal exceeding the setting value is output.

[5] Separately configure the defined interface setting for Clock and XClock.

Note that it may not be possible to select some items, depending on the level guard setting.

ltem	Ampl	Offset	
	Voh	Vol	Vth
Variable	_	_	_
PCML	+3.3 V	+2.8 V	+3.05 V
NCML	0.0 V	$-0.5 \mathrm{V}$	$-0.25~\mathrm{V}$
SCFL	0.0 V	–0.9 V	$-0.45 \mathrm{V}$
NECL	-0.9 V	–1.7 V	–1.3 V
LVPECL	+2.4 V	+1.6 V	+2.0 V
LVDS (400 mV)	+1.4 V	+1.0 V	+1.2 V

Table 4.3.3-2 Amplitude setting values

[6] Separately set the amplitude for Clock and XClock. The setting range varies with the Level Guard, and Offset settings and the installed options. The amplitude setting ranges when Defined Interface is set to Variable are shown in the table below.

Option installed into MU18202xA	Amplitude	Setting steps
None	Min. 0.3 Vp-p, Max. 1.0 Vp-p (Fixed)	_
With MU182020A-x02 MU182021A-x02 installed	Min. 0.7 Vp-p, Max. 1.0 Vp-p (Fixed)	_
With MU182020A-x21 MU182021A-x21 installed	0.5 to 2.0 Vp-p	0.002 V

Table 4.3.3-3 Amplitude setting range

[7] Separately set the offset for Clock and XClock.

The setting range varies depending on the level guard setting and amplitude setting. The following shows the settable Amplitude range when Defined Interface it set to Variable. In addition, when [AC OFF] is pressed, [AC ON] is set and the output is AC-coupled.

Table 4.3.3-4 Offset setting range

Option installed into MU18202xA	Offset	Setting steps
With MU182020A-x21 installed	-4.0 to 3.3 V	0.001 V
With MU182021A-x21 installed	-4.0 to 3.3 V	0.001 V

- [8] Separately set the external ATT factor for Clock and XClock. When a fixed attenuator is connected to the Clock/XClock output connector of the MU181020A, the attenuation of the attenuator is added to the value for the DUT and displayed. A value from 0 to 40 dB can be set in 1-dB steps. When Defined Interface is not set to Variable, the setting is reset to 0 and becomes invalid. Values displayed in the External ATT Factor-Amplitude and Offset display areas indicates the amplitude and offset value after passing through the attenuator, respectively.
- [9] Set the Duty for both Clock and XClock.

Table 4.3.3-5Duty setting range

Option installed into MU18202xA	Duty setting range	Setting steps
With MU182020A-x21 installed	-25 to 25 V	1
With MU182021A-x21 installed	-25 to 25 V	1

[10] Set input clock band switching.

When outputting data at twice the input clock, select [Half Rate Clock]. When outputting data at the same rate as the input clock, select [Full Rate Clock].

If the MU182020A-x02 or MU182021A-x02 is not installed, operate at [Half Rate Clock]. Moreover if neither the MU182020A-x02/x21 nor the MU182021A-x20/x21 module is installed, [Clock Interface] is not displayed and operation is only at the [Half Rate Clock] rate.

Notes:

- 1. The DUT may be damaged if the output setting is configured incorrectly. To prevent damage to the DUT, confirming the interface condition with the DUT, or configuring the level guard setting before making the output setting is recommended.
- 2. When PCML, LVPECL, or NECL is selected for Defined Interface, the voltage corresponding to the DUT's termination voltage is applied to the output side of the MU181020A. In this event, the DUT may be damaged if the interface conditions do not match. Be sure to confirm the interface conditions.
- 3. Waveforms may be distorted (what is known as a ringing phenomenon) when a commercially available ECL terminator is used to observe output waveforms. This is, however, caused by the characteristics of the ECL terminator; the waveform output from the mainframe is not distorted.
- 4. The current for the output part is limited (50 mA for sourcing current and 80 mA for sinking current) for protection. If an over-current flows due to the wrong interface condition, the offset voltage for an observed waveform may therefore not reach the set level.
- 5. Be sure to confirm that a fixed attenuator is connected between the MU181020A and the DUT before setting the external ATT factor. If the external ATT factor is set when no fixed attenuator is connected or when the fixed attenuator has an attenuation value less than that set in the External ATT Factor area, the DUT may be damaged.

6. Immediately after changing the frequency of the reference signal generator from a high frequency to a low frequency, the amplitude may increase temporarily about 30%, then settled down to a specified value.

If it exceeds the rated value of the DUT, turn OFF the Output of MP1800A prior to change of the frequency first, and then turn ON the Output after the frequency change.

4.3.4 Setting Emphasis

When the MU182021A-x40 is installed and a Power Divider is connected externally, an emphasis signal can be generated downstream of the Power Divider.

[Emphasis Control] is only enabled when the MU182021A-x40 Emphasis option is installed *and* the Combination Setting status is 25G Channel Synchronization.

The Emphasis generation principle is shown in Figure 4.3.4-1.



Fig. 4.3.4-1 Emphasis Generation Principle



Fig. 4.3.4-2 Emphasis tab window

[1] Select ON/OFF for Emphasis output.

When ON is set, the [Data1 Interface] and [Data2 Interface] tab setting items are restricted and the Emphasis signal is output. At this setting, the [Data1 Interface] and [Data2 Interface] tab settings are disabled.

Note:

1. When the Level Guard setting at the [Data1 Interface] and [Data2 Interface] tabs is ON, the following dialog message is displayed to set the Level Guard function to OFF.

- 2. When the Defined Interface setting at the [Data1 Interface] and [Data2 Interface] tabs is other than Variable, the following dialog message is displayed to set the setting to Variable.
- 3. When the Tracking setting at [Data1 Interface] and [Data2 Interface] tabs is set to ON, the following dialog message is displated to set the setting to OFF.
- 4. Dialog message: Change the Tracking and Level Guard settings to OFF and the Defined Interface settings to Variable.
- [2] As the default Tracking value is ON, the setting values of Amplitude, Emphasis Amplitude Ratio, Offset, External ATT Factor of XData will be the same as the Data. If setting is performed individually, disable Tracking for configuration.
- [3] Set the amplitude for both Data, and XData. The setting range varies according to the Emphasis Amplitude Ratio, External ATT Factor, and installed data output options.
 Figure 4.3.4-3,4 shows the concept for the emphasis output setting. In addition, the Amplitude calculation is displayed based on the following equation.
 - a) When Emphasis Amplitude Ratio is negative value Amplitude(B)=(Data1 Amplitude+Data2 Amplitude)/2
 - b) When Emphasis Amplitude Ratio is positive value Amplitude(B)=(Data1 Amplitude-Data2 Amplitude)/2

Emphasis Pulse Width



Fig. 4.3.4-3 Emphasis output setting image (if negative)



Fig. 4.3.4-4 Emphasis output setting image (if positive)

[4] Set the Emphasis Amplitude Ratio for both Data, and XData. The setting range varies with the Amplitude, External ATT Factor, and installed data output options. Pressing the +/- button will show the output waveforms like the images in Fig. 4.3.4-3 and Fig. 4.3.4-4. The Emphasis Amplitude Ratio calculation is displayed based on the following equation.

Emphasis Amplitude Ratio=20Log₁₀ (A/B)

A : Voltage displayed in Figure 4.3.4-3,4 Emphasis Amplitude Ratio

- B : Voltage displayed in Figure 4.3.4-3,4 Amplitude
- [5] Set the External ATT Factor for each of Data1, XData1, Data2, and XData2. When a fixed attenuator is connected externally to each of the Data1, XData1, Data2, and XData2 connectors, various types of emphasis signal can be set by taking into account the value of the fixed attenuator.

The default setting value is 3 dB for Data1 and Data2, and 10 dB for XData1 and XData2.

The setting range is 0 to 40 dB in 1-dB steps.

- [6] Set the offset for Data, and XData. The setting range varies depending on External ATT Factor. In addition, when [AC OFF] is pressed to set [AC ON], the output is AC coupled. The low cutoff frequency is about 100 kHz.
- [7] Set the Emphasis Pulse Width. The Emphasis Pulse Width can be varied as shown in Figure 4.3.4-3. Emphasis Pulse Width: -500 to 1500 mUI/2-mUI steps Either mUI or ps units can be set.
- [8] The emphasis output phase can be changed relative to the clock output. See section 4.3.2 for the Delay setting. Delay setting range for Emphasis output: -2000 to + 2000 mUI

Notes :

- 1. The DUT may be damaged if the output setting is configured incorrectly. To prevent damage to the DUT, confirming the interface condition with the DUT.
- 2. Be sure to confirm that a fixed attenuator is connected between the MU182020A and the DUT before setting the external ATT factor. The DUT may be damaged due to the increased actual output amplitude if not connected to a fixed attenuator or when connected to a fixed attenuator with an attenuation value smaller than that set by External ATT Factor.
- 3. When used in combination with an external Power Divider, sometimes there may be excessive waveform distortion or jitter caused by reflection, etc. This can be mitigated by connecting an external attenuator.
- 4. When using the emphasis function, we recommend using the external Power Divider and cable supplied with the emphasis accessories.
- 5. For Amplitude , Emphasis Amplitude Ratio , Offset , and Ext.ATT Factor, the values set first will take precedencee. Therefore, the setting range varies depending on its respective setting value.

4.4 Setting Test Patterns

The data patterns output by this equipment are determined by the Combination setting (see section 4.5), and by the pattern setting of the MU181020A/B Pulse Pattern Generator. When Combination is set, the pattern selected at the MU181020A/B Operation screen becomes the multiplexed pattern output from this equipment.

Patterns setting is performed at the [Pattern] Tab of the MU181020A/B Operation screen.

For the setting method, refer to the MU181020A/B operation manual.

[1:1:1]12.5Gbit/s1	PPG
Output Pattern	Error Addition Misc
- Test Pattern -	RBS -Logic-POS -Bit Shift-1bit -
Length	2^15-1 💌 bits
Mark Ratio	1/2 •

Fig. 4.4-1 Pattern tab window

4.5 Multi Channel Function

Multi-channel sync operation is performed by installing multiple MU181020A/B Pulse Pattern Generator boards in the MP1800A. Multi-channel functions include the Combination and Channel Synchronization functions.

Combination Function Types

- (1) 4ch Combination: when four PPG/ED modules installed
- (2) 25Gx2ch Combination: when four PPG/ED modules installed
- (3) 2ch Combination: when two or more PPG/ED modules installed

Channel Synchronization Function Types

- (1) 12.5G Channel Synchronization: when two or more PPG modules installed
- (2) 25G Channel Synchronization: when four PPG modules installed

4.5.1 Combination Function

When using the Multi Channel function, pattern generation can be synchronized between modules and receiving can be synchronized too. It is possible to evaluate 40G applications by multiplexing a 25G signal using this function.



For combination of 40G 1:4DEMUX

Fig. 4.5.1-1 4 Ch Combination pattern generation/reception


Sync control to receive 25G 2 Ch data using DEMUX



For combination of MU182041A 2ch DEMUX





For combination of MU182040A 1ch DEMUX



Chapter 4 Configuration of Setup Dialog Box







For combination of MU182021A 2ch MUX





Fig. 4.5.1-6 Bit Skew adjustment function

4.5.2 Combination setting

To use the Multi-channel function, click the [Combination Setting] module function button to open the Combination Setting dialog box for setting.

For details, refer to Section 5.3.3 "Combination setting" in the MX180000A Operation Manual.

Combination S	etting		×
	Operation C Independent C Combination C Channel Synchronizatio		OK Cancel
Slot No.	Combination	Name	
	4ch 💌		
Slot 1	2ch	MU182041A 25Gbit/s 2ch DEM	1UX
Slot 2	4ch	MU182041A 25Gbit/s 2ch DEM	4UX
Slot 3	25Gx2ch Combination	MU181040A 12.5Gbit/s ED	
Slot 4	Ach ED	MU181040A 12.5Gbit/s ED	
Slot 5	4ch ED	MU181040A 12.5Gbit/s ED	
Slot 6		MU181040A 12.5Gbit/s ED	

Fig. 4.5.2-1 Combination Setting dialog box

Chapter 4 Configuration of Setup Dialog Box

	Table 4.6.2-1 Octeon Layout of Combination Cetting				
	Operation	Settings	Contents		
[1] Independent			Select to operate PPG and ED independently.		
[2]	Combination	2ch	Select when performing 25G tests in combination with this module.		
		4ch	Select when performing 40 tests using external MUX/DEMUX.		
		25Gx2ch Combination	Select when generating/receiving 25G 2 Ch data in combination with this module.		
	Channel Synchronaization	12.5G CH Sync	Select when always outputting with synchronized header bit for PON applications, etc.		
		25G CH Sync	Select when always outputting with synchronized header bit between two 25G channels.		

Table 4.5.2-1	Screen Lay	out of Comb	ination Setting
---------------	------------	-------------	-----------------

Confirm the selected operation by pressing the [OK] button.

Chapter 5 Use Example

This chapter provides use examples of measurement using the MU182020A/21A.

- 5.1 Measuring Optical Transceiver Module 5-2
- 5.2 DQPSK Transmission Test...... 5-6

5.1 Measuring Optical Transceiver Module

This section explains how to measure 25G optical devices using the MP1800A.

This measurement is explained using a test setup with one MU182040A module, two MU181020A/B Modules, and two MU181040A/B modules installed in the MP1800A.

The options configuring the test system are as follows:

MP1800A-016:1 module MU181020A/B-002/x11/x30:2 modules MU182020A-x01/x02/x13/x31:1 module MU181040A/B-002/x30:2 modules MU182040A-x01/x02/x31:1 module MG3693B:1 module

- 1. Connect the GND of the MP1800A and that of the DUT.
- 2. Connect the power cables.
- 3. Turn on the MP1800A, and set the measurement conditions as follows.
 - Connect MP1800A, MU181020A/B, MU182020A, MU181040A/B, MU182040A, and MG3693B Signal Generator (hereafter, MG3693B), referring to Fig. 5.1-1.
 - (2) When connecting this equipment and the MU181020A/B, the two MU181020A/B modules must be synchronized. (This equipment requires synchronization of the four MU181020A/B modules when using the MU182021A.)
 In addition, when connecting MU182040A and MU181040A/B, the two MU181040A/B modules must be synchronized. (This equipment requires synchronization of the four MU181040A/B when using the MU182041A.)
 Press the [Combination] button for the module function and select 2 Ch Combination.
 - (3) Adjust the data output interface of the MU182020A to the input interface of the DUT. The output is already OFF at this time.
 - (4) Set a test pattern for the sender side. The test pattern is selected at the MU181020A Pattern screen. Changing the setting for one channel of the MU181020A/B is reflected in the settings for all channels.

(5)	Set the operation bit rate at the MG3693B.
	When the DUT requires a 1/1 Clock frequency, set the 1/1
	operation rate at the MG3693B.
	When the DUT requires a $1/1$ Clock frequency, set the $1/2$
	operation rate at the MG3693B.
	The Clock Input Band SW at the Clock Interface Tab is
	switched according to the input operation rate.

- (6) Match the MU182040A data input interface to the DUT output. Set the termination and threshold conditions at the MU182040A Data Interface screen.
- (7) Set the test pattern for the received side. The test pattern is selected at the MU181040A/B Pattern screen. Changing the setting for one channel of the MU181040A/B is reflected in the settings for all channels.
- (8) Set the operation rate for the clock input to the MU182040A External Clock Input connector. The Clock Input Band SW at the Data Interface Tab is switched according to the input operation rate.
- (9) After all parameters have been set, turn off the MP1800A.
- 4. Connect the MP1800A and the DUT.

Use the accessory coaxial cables or equivalent coaxial cables to connect the input and output signals.

Note :

At this time, short the cable cores, using a thin pointed metal stick such as tweezers before connection. See Fig. 5.1.1-1 for connection of the instruments.

Check that the output level (O/E) of the DUT is appropriate for the MU182040A data input range. If it is out of range, adjust the level using an attenuator.

Chapter 5 Use Example



Fig. 5.1-1 Connection diagram for XFP module evaluation

5. Turn on the MP1800A first, and then DUT.



The DUT may be damaged if a signal line is connected or disconnected while the output is ON. Be sure to turn off the MP1800A before changing the cable connection.

- 6. Enable the signal output of the MU182020A.
 Set the Output of MG3693B and Data/XData Output in the Data Interface screen to ON.
 Then, set [Output ON/OFF] of the module function button or [Output] of the MP1800A front panel to ON.
- 7. Set the threshold voltage and phase of MU182040A. When the Auto Adjust function is used, clicking the Auto Adjust module function button on the menu bar automatically adjusts the threshold voltage to the optimum value for the DUT.
- 8. Start measurement. The BER measurement results can be checked at the Result screen.
- 9. Confirm that the DUT operates normally. If so, DUT (E/O) sensitivity measurement can be performed for the DUT by adjusting the output level of the MU182020A.

5.2 DQPSK Transmission Test

This section describes how to perform 25 Gbit/s DQPSK transmission test using MP1800A.

This measurement describes a test example with the configuration where MU181020A/B, MU182041A, MU181040A/B, and this equipment are installed in MP1800A as a reference. The options configuring the test system are as follows:

MP1800A-016:2 modules MU181020A/B-002/x11/x30:4 modules MU182021A-x01/x02/x13/x31:1 module MU181040A/B-002/x30:4 modules MU182041A-x01/x02/x31:1 module MG3693B:1 module

- 1. Connect the GND of the MP1800A, device under test (DUT).
- 2. Connect the power cables.
- 3. Turn on the MP1800A on which the MU181020A modules are mounted, and set the measurement conditions as follows.
 - Connect MP1800A, MU181020A/B, MU182021A, MU181040A/B, MU182041A, and MG3693B, referring to Fig. 5.1-1.
 - (2) When connecting this equipment and the MU181020A/B, the four MU181020A/B modules must be synchronized. In addition, when connecting MU181040A/B and MU181041A, the four MU181040A/B modules must be synchronized. Press the [Combination] button for the module function and select 25G x 2 Ch Combination.
 - (3) Match the data output interface of this equipment to the input of the DUT (DQPSK Precoder). The output is already off at this time.
 - (4) Set the test pattern for the send side.Select a test pattern at the MU181020A/B Pattern screen.Changing the setting for one channel of the MU181020A/B is reflected in the settings for all channels.
 - (5) Set the operation bit rate at the MG3693B. When generating a CSRZ signal, set a 1/2 operation rate at the MG3693B. Set Clock Input Band SW in the Clock Interface screen of this equipment to Half Rate Clock (when generating an RZ signal, set a 1/1 operation rate for the MG3693B, and set Clock Input Band SW to Full Rate Clock.).

- (6) Match the clock output interface to the input of the DUT (Driver AMP driving the LN Modulator used for CSRZ generation). The Output is already set to off at this time.
- (7) Set the reception test pattern. Select the test pattern from the Pattern screen of MU181040A/B. Changing the setting of one channel of MU181040A will reflect the setting in all channels.
- (8) Set the operation rate of Clock to be input to External Clock Input of MU182041A. Clock Input Band SW in the Data Interface screen is toggled in accordance with the input operation rate.
- (9) When setting the parameters completely, turn off the MP1800A and MG3693B.
- 4. Connect the MP1800A and the DUT.

Connect the I/O signals, using the supplied coaxial cables (cables equivalent to the supplied ones can also be used). At this time, short the cable cores, using a thin pointed metal stick such as tweezers before connection.

See Fig. 5.2-1 for connection of the instruments.

Check whether the output level of the DUT (CSRZ-DQPSK Encoder Module) is conformed to the input data range of this equipment or not. When it is not conformed, adjust the level using an attenuator.

Chapter 5 Use Example



Fig. 5.2-1 CSRZ-DQPSK Modulator connection diagram

5. Turn on the MP1800A first, and then the DUT.

CAUTION A

The DUT may be damaged if a signal line is connected or disconnected while the output is ON. Be sure to turn off the MP1800A before changing the cable connection.

- 6. Enable the signal output of the MU182020A.
 Set Output of MG3693B and Data/XData Output in the Data Interface screen to ON.
 In addition, set Clock/XClock Output of the Clock Interface screen to ON.
 Last, set the [Output] button of the module function buttons to ON.
- Set the Delay for Data1 and Data2.
 When isolating the LN Modulator used for the DUT CSRZ Signal and I/Q signal modulation, adjust the values of Data1 and Data2 so that the final output waveform is the same as the CSRZ Signal waveform.
- 8. Set the threshold voltage and phase of MU182041A. Clicking [Auto Adjust] of the module function button will always automatically set the optimum position with respect to the DUT.
- Start the measurement. The BER measurement results can be confirmed in the Result screen of MU182041A.
- 10. After confirming that the DUT (transmission section/reception section) is operating normally, it is possible to perform transmission test by the CSRZ-DQPSK signal if the test object (such as Fiber) is placed between transmission section and reception section.

Chapter 6 Performance Test

This chapter describes the performance testing of the MU182020A/21A.

6.1	Overvi	ew	6-2
6.2	Devices Required for Performance Tests		
6.3	Perfor	mance Test Items	6-4
	6.3.1	Operating frequency range	6-4
	6.3.2	Waveform evaluation test	6-7

6.1 Overview

Performance tests are executed to check that the major functions of the MU182020A/21A meet the required specifications. Execute performance tests at acceptance inspection, operation check after repair, and periodic (once every six months) testing.

6.2 Devices Required for Performance Tests

Before starting performance tests, warm up the MU182020A/21A and the measuring instruments for at least 30 minutes. Table 6.2-1 shows the devices required for performance tests.

Device Name	Requi	red Performance
Error detector + DEMUX (MP1800A-015/016 +MU18204xA +2 MU181040A/B units)	Operating frequency: Data input sensitivity:	8 to 25 GHz 100 mVp-p or more
Error detector + DEMUX (MP1800A-015/016 +MU18204xA-x01 +2 MU181040B units)	Operating frequency: Data input sensitivity:	8 to 28 GHz 100 mVp-p or more
Signal generator (MG3693B)	Operating frequency: Output amplitude:	2 to 30 GHz 0.3 to 1.0 Vp-p
Sampling Oscilloscope	Band frequency: 70 GHz or more	

Table 6.2-1 Devices required for performance test

Note:

Before starting the performance tests, warm up the device under test and the measuring instruments for at least 30 minutes and wait until they become sufficiently stabilized, unless otherwise specified. Additional conditions are required for maximum measurement accuracy: measurements must be performed at room temperature, fluctuations of AC power supply voltage must be small, and noise, vibration, dust, and humidity must be insignificant.

6.3 Performance Test Items

This section describes the following test items.

- (1) Operating frequency range
- (2) Waveform

6.3.1 Operating frequency range

(1) Specifications

Table 6.3.1-1 Specifications

Madal	Options		Specifications
Woder	x01	x02	Specifications
MU182020A/21A	No	No	4 to 12.5 GHz
	Yes	No	4 to 14 GHz
	No	Yes	At Full Rate Clock:8 to 25 GHz When selecting Half Rate Clock:4 to 12.5 GHz
	Yes	Yes	When selecting Full Rate Clock:8 to 28 GHz When selecting Half Rate Clock:4 to 14 GHz

(2) Device connection



Fig. 6.3.1-1 Connection diagram for operating frequency range test

- (3) Test procedure
 - 1. Connect each measuring instrument using cables as shown in Fig. 6.3.1-1.

- 2. Install this module in the MP1800A and switch on the power. Switch on the power of the MP1800A and each measuring instrument and allow them to warm up.
- 3. Set the output level so as not to overload the input to the 25G DEMUX.

- 4. Press the [Combination] button for the module function and select 25G x 2 Ch Combination.
- 5. Set the Data signal output amplitude of the MU181020A to 500 mVp-p, offset (Vth) to 0 V, MU181020A test pattern to PRBS 31, and Mark Ratio to 1/2. Set the Error Detector test pattern in the same way.
- 6. Set the MP1800A signal output to ON to output the signal.
- 7. Adjust the MU18204xA phase and threshold to the optimum values. (Use the auto search function.)
- 8. Check that no error is detected by the MU181040A/B.
- 9. Change the operating frequency and check if no error occurs within the rated operating frequency range.

6.3.2 Waveform evaluation test

(1) Specifications

Option	Specifications	
MU182020A-x10	Amplitude : 0.25 V to 1.75 Vp-p	
Variable Data	Offset : -2.0 to $+3.3$ Voh	
Output (0.25 to	Cross Point : 20 to 80%	
1.75 Vp-p) Retrofit	Tr/Tf:Typ.12 ps(20 to 80%)@25 Gbit/s, 1.75 Vp-p	
1 1	Total Jitter : Typ. 8 psp-p*	
	Waveform distortion : Typ. $\pm 25 \text{ mV} \pm 10\%@25 \text{ Gbit/s}$	
MU182020A-x11	Amplitude : 0.25 to 2.50 Vp-p	
Variable Data	Offset : -2.0 to $+3.3$ Voh, Min. -4 Vol	
Output (0.5 to 2.5	Cross Point : 20 to 80%	
Vp-p) Retrofit	Tr/Tf:Typ.12 ps(20 to 80%)@25 Gbit/s, 2.5 Vp-p	
1 1	Total Jitter : Typ. 8 psp-p*	
	Waveform distortion : Typ. ±25 mV ±10%@25 Gbit/s	
MU182020A-x13	Amplitude : 0.5 to 3.5 Vp-p	
Variable Data $Offset : -2.0 \text{ to } +3.3 \text{ Voh}, \text{ Min. } -4 \text{ Vol}/$		
Output (0.5 to 3.5 Cross Point : 20 to 80%		
Vp-p) Tr/Tf : Typ.12 ps(20 to 80%)@25 Gbit/s, 3.5 Vp-p		
	Total Jitter : Typ. 8 psp-p*	
	Waveform distortion : Typ. $\pm 25 \text{ mV} \pm 10\% @25 \text{ Gbit/s}$	

*: The jitter specification value is defined assuming use of an oscilloscope with residual jitter of less than 200 fs (RMS).

Chapter 6 Performance Test



(2) Device connection

Fig. 6.3.2-1 Connection diagram for waveform test

- (3) Test procedure
 - 1. Connect the cables among the measuring instruments, referring to Fig. 6.3.2-1.
 - 2. Install the MU181020A in the MP1800A, and turn on the MP1800A. Set the power of the MP1800A and each measuring instrument to on and allow them to warm up.
 - 3 Press the [Combination] button for the module function and select 2 Ch Combination.
 - 4. Set the Amplitude, Offset, and Cross Point of the output test data at the setting screen.
 - 5. Set the test pattern in the MU181020A/B Pattern tab window. Since the specification parameters are evaluated by observing an Eye pattern, set the test pattern to PRBS 31, and the mark ratio to 1/2.
 - Configure the trigger signal setting. Select 1/N Clock in the AUX Output area on the MU181020A/B Misc tab window, and set the division ratio according to the sampling oscilloscope used.
 - 7. When output of the signal generator and MP1800A signal is set to ON, signal is output.
 - 8. Observe the output waveform on the sampling oscilloscope, and check that all the items conform to the specifications.

This chapter describes the maintenance of the MU182020A/21A.

7-2
7-3
7-3
7-4

7.1 Daily Maintenance

- Wipe off any external stains with a cloth damped with diluted mild detergent.
- Vacuum away any accumulated dust or dirt with a vacuum cleaner.
- Tighten any loose parts fixed with screws, using the specified tools.

7.2 Cautions on Storage

Wipe off any dust, soil, or stain on the MU182020A/21A prior to storage. Avoid storing the MU182020A/21A in any of the following locations:

- Where there is direct sunlight
- Where there is dust
- Where humidity is high and dew may accumulate
- Where chemically active gases are present
- Where the MU181020A may become oxidized
- Where strong vibrations are present
- Under either of the following temperature and humidity conditions: Temperature range of \leq -20°C or \geq 60°C Humidity range of \geq 85%

Recommended storage conditions

In addition to the abovementioned storage cautions, the following environment conditions are recommended for long-term storage.

- Temperature range of 5 to $30^{\circ}C$
- Humidity range of 40 to 75%
- Slight daily fluctuation in temperature and humidity

7.3 Transportation

Use the original packing materials, if possible, when packing the MU182020A/21A for transport. If you do not have the original packing materials, pack the MU182020A/21A according to the following procedure. When handling the MU182020A/21A, always wear clean gloves, and handle it gently so as not to damage it.

<Procedure>

- 1. Use a dry cloth to wipe off any stain or dust on the exterior of the MU182020A/21A.
- 2. Check for loose or missing screws.
- 3. Provide protection for structural protrusions and parts that can easily be deformed, and wrap the MU182020A/21A with a sheet of polyethylene. Finally, cover with moisture-proof paper.
- 4. Place the wrapped MU182020A/21A into a cardboard box, and tape the flaps with adhesive tape. Furthermore, store it in a wooden box as required by the transportation distance or method.
- 5. During transportation, place it under an environment that meets the conditions described in Section 7.2 "Cautions on Storage".

7.4 Calibration

Regular maintenance such as periodic inspections and calibration is essential for the Signal Quality Analyzer Series for long-term stable performance. Regular inspection and calibration are recommended for using the Signal Quality Analyzer Series in its prime condition at all times. The recommended calibration cycle after delivery of the Signal Quality Analyzer Series is twelve months.

If you require support after delivery, contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the CD version.

We may not provide calibration or repair if any of the following cases apply.

- Seven or more years have elapsed after production and parts for the instrument are difficult to obtain, or it is determined that reliability cannot be maintained after calibration/repair due to significant wear.
- Circuit changes, repair, or modifications are done without our approval.
- It is determined that the repair cost would be higher than the price of a new item.

7.5 Disposal

Confirm the notes described in the Signal Quality Analyzer Series Installation Guide and observe national and local regulations when disposing of the MU182020A/21A.

Chapter 8 Troubleshooting

This chapter describes how to check whether a failure has arisen when an error occurs during the operation of the MU182020A/21A.

8.1	Problems Discovered during	
	Module Replacement	8-2
8.2	Problems Discovered during	
	Output Waveform Observation	8-2
8.3	Problems Discovered during	
	Error Rate Measurement	8-4

8.1 Problems Discovered during Module Replacement

Table 8.1-1 Remedies for problems discovered during replacement of MU182020A/21A module

Symptom	Location to Check	Remedy
A module is not recognized.	Is the module installed properly?	Install the module again by referring to Section 2.3 "Installing and Removing Modules" in the installation guide.
	Are the appropriate modules installed?	To check the appropriate modules and software version of the MU182020A/21A, access to "MP1800 Series Signal Quality" on your Web site (<u>http://www.anritsu.com</u>). Right-click the "MP1800 Series Signal Quality" and you can access to your area website. If the appropriate modulus are not recognized, it may have failed. Contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the CD version.

8.2 Problems Discovered during Output Waveform Observation

 Table 8.2-1
 Remedies for problems discovered during waveform observation

Symptom	Location to Check	Remedy	
Output waveform cannot be monitored normally.	Is the [Data/XData] or [Clock/XClock] on the Output tab window set to ON?	In the Output tab window, set [Data/XData] or [Clock/XClock] to be output to ON. When the module function button [Output ON/OFF] is enabled, click it to set to ON.	
	Is module function button [Output ON/OFF] is set to ON?	Click the module function button [Output ON/OFF] to ON.	
	Is the operating clock supplied normally?	Check that the bit rate can be monitored using the frequency from the signal generator and the Clock Input Band Switch setting. When the clock is supplied externally, check the connection interface. Refer to Section 3.1 "Panel Layout" for the interface.	
	Is the trigger clock set correctly?	It is recommended to use the signal output from AUX output connector as the trigger clock. Check the AUX output connector settings and interface with the sampling oscilloscope to be measured.	
	Is the electrical interface cable loose?	Tighten the connector.	

8.2 Problems Discovered during Output Waveform Observation

Symptom	Location to Check	Remedy
Output waveform cannot be monitored normally. (continued)	Do the cables used have good high-frequency characteristics?	Use cables or connectors with good high-frequency characteristics.
	Are the connection cables between this module and the MU181020A/B connected correctly?	Connect the cables between this module and the MU181020A/B as described in chapter 3 in the correct sequence.
	Is the electrical interface between this module and the MU181020A/B matched?	When using a separate mainframe, match the electrical interface to satisfy the specifications in chapter 1 and adjust Delay.1
	Are the cables between the 1/2 Clock Output connector of this module and the MU181020A/B the same length?	The cables between the 1/2 Clock Output connector of this module and the MU181020A/B are the same length.
Are the cables between the MU181020A/B Data Output and Clock Output and between the 1/2 Data Input and 1/2 Clock Input connectors of this module the same length?		The cables between the 1/2 Clock Output connector of this module and the MU181020A/B are the same length.

Table 8.2-1 Remedies for problems discovered during waveform observation (Cont'd)

8.3 Problems Discovered during Error Rate Measurement

 Table 8.3-1
 Remedies for problems discovered during error rate measurement

Symptom	Location to Check	Remedy		
An error occurs.	Is the connection interface with the DUT to be measured correct?	Check that the data rate, level, offset termination conditions are the same.		
	Is the logic pattern of the mainframe (or the MU181020A/B) and the MU18204xA (or the MU181040A/B) set correctly?	Check that the pattern generated by this module can be received by the DUT, and that the settings for the pattern generated by the DUT and the MU18204xA (or MU181040A) detection pattern are matched. If the DUT outputs the patterns from the MU181020A as they are, connect the MU181020A and ED directly to check if an error is detected.		
	Were the cables between this module and the MU181040A/B connected in the correct sequence?	Connect the cables between this module and the MU181040A/B correctly as described in section 3.2 Connecting modules.		
	Is the error addition function set to off?	Check that the [Error Addition] switch on the Error Addition screen is set to off.		
	Is the electrical interface cable loose?	Tighten the connector.		
	Do the cables used have good high-frequency characteristics?	Use cables or connectors with good high-frequency characteristics.		
	Are sufficient phase margin and bias margin are secured?	Adjust the phase and offset to be optimal between the MU182020A and the DUT as well as between the DUT and ED, respectively.		

If a problem cannot be solved using any of the items listed above, perform initialization and check the items again. If the problem still occurs, contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the CD version.

Appendix

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Appendix

A.1 List of Initialized Settings

This appendix shows the MU182020A/21A settings that are initialized to the defaults at factory shipment.

In addition, All settings can be initialized using the Initialize pull-down from the File menu.

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Output	Data/XData Outp	out ON/OFF		ON
Data	Clock ON/OFF (MU182020A-x21	,MU182020A-x02)		ON
	Amplitude Offset			Vth
	Data/XData	Tracking		OFF
		Level Guard		OFF
		Level Guard	Amplitude	1.750 Vp-p (MU182020A-x10)
		Setup		2.500 Vp-p (MU182020A-x11)
				3.500 Vp-p (MU182020A-x13)
			Offset limit	-3.750 to 3.300 V (MU182020A-x10)
				-4.000 to 3.300 V
				(MU182020A-x11)
				-4.000 to 3.300 V
				(MU182020A-x13)
		Defined	A 11. 1	Variable
		Interface	Amplitude	1.000 Vp-p
			Offset switching	ACOFF
			Offset	0.000 V
			External ATT Factor	0 dB
		Cross Point		50%
		Half Period Jitt	ter	0
		Delay		0 mUI (MU182020A-x30, MU182020A-x31)
			Calibration	– (MU182020A-x30, MU182020A-x31)
			Jitter Input	OFF (MU182020A-x30, MU182020A-x31)
			Delay Relative	OFF (MU182020A-x30, MU182020A-x31)

 Table A.1–1
 List of Initialized Items for MU182020A

Appendix A List of Initial Settings

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Output	Clock/XClock	Tracking		OFF
Data	(MU182020A-	Level Guard		OFF (MU182020A-x21)
(continued)	x21)	Level Guard Setup	Amplitude	2.000 Vp-p
			Offset limit	-4.000 to 3.300 V
		Defined Interface		Variable
			Amplitude	1.000 Vp-p
			Offset switching	AC OFF (MU182020A-x21)
			Offset	0.000 V (MU182020A-x21)
			External ATT	0 dB (MU182020A-x21)
			Factor	
		Duty		0 (MU182020A-x21)

Table A.1–1 List of Initialized Items for MU182020A (Cont'd)

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Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Output	Data/XData Output ON/OFF			ON
Data1,2	Clock/XClock Out (MU182021A-x21	put ON/OFF .,MU182021A-x02	2)	ON
	Amplitude Offset			Vth
	Data/XData	Data1,2 Tracking		OFF
		Tracking		OFF
		Level Guard		OFF
		Level Guard Setup	Amplitude	1.750 Vp-p (MU182021A-x10) 2.500 Vp-p (MU182021A-x11)
			Offset limit	3.500 Vp-p (MU182021A-x13) -3.750 to 3.300 V (MU182021A-x10)
				-4.000 to 3.300 V (MU182021A-x11)
				-4.000 to 3.300 V (MU182021A-x13)
		Defined		Variable
		Interface	Amplitude	1.000 Vр-р
			Offset switching	AC OFF
			Offset	0.000 V
			External ATT Factor	0 dB
		Cross Point		50%
		Half Period Jitter		0
		Delay		0 mUI (MU182021A-x30, MU182021A-x31)
			Calibration	– (MU182021A-x30, MU182021A-x31)
			Jitter Input	OFF (MU182021A-x30, MU182021A-x31)
			Delay Relative	OFF (MU182021A-x30, MU182021A-x31)

Table A.1–2 List of Initialized Items for MU182021A

Appendix A List of Initial Settings

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Output	Clock/XClock	Tracking		OFF (MU182021A-x21)
Data1,2	(MU182021A-	Level Guard		OFF (MU182021A-x21)
(continued)	x21)	Level Guard Setup	Amplitude	2.000 Vp-p
			Offset limit	-4.000 to 3.300 V
		Defined Interface		Variable (MU182021A-x21)
			Amplitude	1.000 Vp-p (MU182021A-x21)
			Offset switching	AC OFF (MU182021A-x21)
			Offset	0.000 V (MU182021A-x21)
			External ATT Factor	0 dB (MU182021A-x21)
		Duty		0 (MU182021A-x21)

 Table A.1–2
 List of Initialized Items for MU182021A (Cont'd)

Note:

When the Initialize function is executed in Combination or Channel Synchronization status, Independent, which is the initial status, is restored.
Appendix B Setting Restrictions

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B.1 Setting range of offset and amplitude

■ Relationship between offset reference value and amplitude



Fig. B.1-1 Relationship between offset reference value and amplitude

B.1.1 MU182020/21A-x10 Variable Data Output (0.25 to 1.75 Vp-p)

<Specification> Amplitude: 0.25 to 1.75 Vp-p Offset: -2.0 to +3.3 V (Voh)

(a) Voh



Fig. B.1.1-1 Setting range of amplitude and offset based on offset reference (Voh) (MU182020/21A-x10)

(b) Vth



Fig. B.1.1-2 Setting range of amplitude and offset based on offset reference (Vth) (MU182020/21A-x10)





Fig. B.1.1-3 Setting range of amplitude and offset based on offset reference (Vol) (MU182020/21A-x10)

B.1.2 MU182020/21A-x11 Variable Data Output (0.5 to 2.5 Vp-p)

<Specification> Amplitude: 0.5 to 2.5 Vp-p Offset: -2.0 to +3.3 V (Voh)

(a) Voh

(b) Vth



Fig. B.1.2-1 Setting range of amplitude and offset based on offset reference (Voh) (MU182020/21A-x11)



Fig. B.1.2-2 Setting range of amplitude and offset based on offset reference (Vth) (MU182020/21A-x11)

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Appendix B Setting Restrictions



Fig. B.1.2-3 Setting range of amplitude and offset based on offset reference (Vol) (MU182020/21A-x11)

B.1.3 MU182020/21A-x13 Variable Data Output (0.5 to 3.5 Vp-p)

<Specification> Amplitude: 0.05 to 3.5 Vp-p Offset: -2.0 to +3.3 V (Voh)

(a) Voh



Fig. B.1.3-1 Setting range of amplitude and offset based on offset reference (Voh) (MU182020/21A-x13)

(b) Vth



Fig. B.1.3-2 Setting range of amplitude and offset based on offset reference (Vth) (MU182020/21A-x13)

Appendix B Setting Restrictions



Fig. B.1.3-3 Setting range of amplitude and offset based on offset reference (Vol) (MU182020/21A-x13)

B.1.4 MU182020/21A-x21 Clock Output (0.5 to 2.0 Vp-p)

<Specification> Amplitude: 0.5 to 2.0 Vp-p Offset: -2.0 to +3.3 V (Voh)

(a) Voh



Fig. B.1.4-1 Setting range of amplitude and offset based on offset reference (Voh) (MU182020/21A-x21)



Fig. B.1.4-2 Setting range of amplitude and offset based on offset reference (Vth) (MU182020/21A-x21)

Appendix B Setting Restrictions



Fig. B.1.4-3 Setting range of amplitude and offset based on offset reference (Vol) (MU182020/21A-x21)

B.2 Combination Function Configuration

The conditions required to execute the Combination function by using multiple MU181020A/B modules are described below.

All of the following conditions must be satisfied to execute the Combination function.

Enabling conditions for Combination function

- Two or more MU181020A/B modules are mounted in one mainframe. (To be mounted from the top slot 1 in order)
- Do not mix MU181020A and MU181020B modules. In addition, do not mix options (MU181020A-x10/11x/12/x13/ and MU181020B-x/11x/12/x13).
- Installed modules must be either all MU181020A-002 modules or all MU181020B-002 modules.
- Installed modules must be either all MU181020A-x30 modules or all MU181020B-x30 modules.
- All or none of the inserted MU181020A/B modules must have MU181020A-x21 and MU181020B-x21 installed therein.
- The mainframe option is either MP1800A-015 or MP1800A-016.

In addition, the following restriction is added for the Combination function.

Restriction for Combination function

• The Alternate, Mixed-Alternate and Sequence patterns cannot be used as the test pattern.

B.3 Channel Synchronization Function Configuration

The conditions required to execute the Channel Synchronization function by using multiple MU181020A/B modules are described below.

All of the following conditions must be satisfied to execute the Channel Synchronization function.

Enabling conditions for Channel Synchronization function

- Two or more MU181020A/B modules are mounted on one mainframe. The MU181020A/B modules that are mounted contiguously starting from Slot 1 are enabled.
- Do not mix MU181040A and MU181040B modules. In addition, do not mix options (MU181020A-x10/11x/12/x13/ and MU181020B-x/11x/12/x13).
 - Installed modules must be either all MU181020A-002 modules or all MU181020B-002 modules.
 - Installed modules must be either all MU181020A-x30 modules or all MU181020B-x30 modules.
 - All or none of the inserted MU181020A/B modules must have MU181020A-x21 and MU181020B-x21 installed therein.

B.4 Combination Operation

When this module and the MU181020A/B are installed in the same mainframe and either 2 Ch Combination or $25G \ge 2$ Ch Combination is selected, operation of this module and the MU181020A/B can be linked (combined).

a) MP1800A-015/016 2ch Combination

Figure B.4-1 shows combined operation of the MU181020A/B in slot1 and slot2 and the MU182020A in slot5 (Data1 for 21A). The Delay setting at the Data Interface tab of this module is linked with the Delay of the MU181020A/B in slot1 and slot2.

The MU181020A/B in slot4 and slot4 and the MU182020A in slot6 are linked (Data2 for 21A).

The Delay setting at the Data Interface tab of this module is linked with the Delay of the MU181020A/B in slot3 and slot4.



Fig B.4-1 MP1800A-015/016 2ch Combination operation

b) MP1800A-015/016 25Gx2ch Combination

Figure B.4-2 shows combined operation of the MU181020A/B in slot1 to slot4 and the MU182020A/21A in slot5 and slot6.





B.5 Settings Common in Combination System

When the MU181040A is used in a Combination system, some setting items will apply to all the other modules in the Combination system.

Table C.3-1 shows whether the setting items are common or independent in a Combination system.

Function	Main Category	Sub-Category	Individual Setting Item	Common/ Independent	
Output	Data/XData Output ON/OFF		tput ON/OFF		
	Clock/XClock Output ON/OFF (MU181020A-x21, MU181020B-x21)			Independent	
	Amplitude Offs	et	Independent		
	Data/XData	Tracking		Independent	
		Level Guard		Independent	
				Independent	
		Level Guard Setup	Amplitude limit	Independent	
			Offset limit	Independent	
				Independent	
			Amplitude	Independent	
		Defined Interface	Offset switching	Independent	
		Offset		Independent	
			External ATT Factor	Independent	
		Cross Point		Independent	
		Delay		Independent	
		Delay	Calibration	Independent	
	Clock/XClock	Tracking		Independent	
	(MU181020A	Level Guard		Independent	
	-x21,	Level Guard Setup	Amplitude limit	Independent	
	MU181020B- v21)		Offset limit	Independent	
	X21/			Independent	
			Amplitude	Independent	
		Defined Interface	Offset switching	Independent	
		Defined interface	Offset	Independent	
			External ATT Factor	Independent	
		Duty		Independent	

 Table B.5-1
 Common/Independent Setting Items in Combination System

B.5 Settings Common in Combination System

Function	Main Category	Sub-Category	Individual Setting Item	Common/ Independent
Pattern	PRBS			Common
		Number of Rows		Common
		Logic		Common (Pattern Common)
		Mark Ratio		Common (Pattern Common)
		Bit Shift		Common
				(Common with Mixed Data)
	Zero-Substit	Number of Rows		Common
	ution	Zero Substitution Le	ngth	Common
		Additional Bit		Common
	Data	Data Pattern		Common
	Mixed Data	Logic		Common (Pattern Common)
		Bit Shift		Common (Common with PRBS)
		Block count		Common
		Row Length		Common
		Data Length		Common
		Row count		Common
		PRBS	Pattern	Common
			Mark Ratio	Common (Pattern Common)
		Scramble		Common
		Scramble Setup		Common
		PRBS Sequence		Common
	Pattern	Zoom		Independent
	Editor	Block count		Common
		Row Length		Common
		Data Length	Data	Common
			Mixed	Common
		Row count		Common
Error	Error			Common
Addition	Addition	Source		Common
		Variation		Common
		Route		Independent
		Error Rate		Common
		When test pattern is	Mixed: Row 1	Common

Table B.5-1 Common/Independent Setting Items in Combination System (Cont'd)

Appendix B Setting Restrictions

Function	Main Category	Sub-Category	Individual Setting Item	Common/ Independent
Misc	Pattern			Common
	Sequence	Repeat	Pulse Width	Common
			Delay	Common
		Burst	Source	Common
			Data Sequence	Common
			Enable Period	Common
			Burst Cycle	Common
			Delay	Common
			Pulse Width	Common
	Aux Input			Common
	Aux Output			Independent
		1/N Clock		Independent
		Pattern Sync	PRBS, Zero Substitution, Data: Position	Independent
			Mixed Data: Block No. Row No.	Independent
		Burst Output 2	Delay	Common
			Pulse Width	Common

Table B.5-1 Common/Independent Setting Items in Combination System (Cont'd)

C.1 Performance Test Record Sheet

Equipment Name: MU182020A 25Gbit/s 1ch MUX MU182021A 25Gbit/s 2ch MUX

Serial No.:

Ambient Temperature: °C

Relative Humidity: %

Option Configuration	Signal Source	Operating Frequency Range Specification	Results
_	Operating Bit Rate	8.0 to 25.0 Gbit/s 8.0 to 28.0 Gbit/s (When MU182020A-x01 is installed)	
MU182020A-x10 (Variable Data Output	Amplitude Setting Error	0.25 to 1.75 Vp-p/2 mV Step Setting Error : ±50 mV ±17% of Amplitude	
(0.25 to 1.75 Vp-p))	Offset Setting Error	2.0 to +3.3 Voh, Min4.0 Vol/1 mV Step Setting Error: ±65 mV ±10% of Offset(Vth) ± (Amplitude Setting Error /2)	
	Cross Point Tr/Tf	20 to 80%/0.1% Step Typ.12ps(20 to 80%) @25 Gbit/s,1.75 Vp-p	
	Total Jitter	Typ. 8psp-p*	
	Waveform Distortion (0-peak)	Typ. ±25 mV ±10%@25 Gbit/s	

Table C.1-1 MU182020A

Option Configuration	Signal Source	Operating Frequency Range Specification	Results
MU182020A-x11 (Variable Data Output	Amplitude Setting Error	0.5 to 2.5 Vp-p/2 mV Step Setting Error : ± 50 mV $\pm 17\%$ of Amplitude	
(0.5 to 2.5Vp-p))	Offset Setting Error	-2.0 to $+3.3$ Voh, Min4.0 Vol/1 mV Step Setting Error: ± 65 mV $\pm 10\%$ of Offset(Vth) \pm (Amplitude Setting Error/2)	
	Cross Point Setting Range	20 to 80% / 0.1% Step	
	Tr/Tf	Typ.12ps(20 to 80%)@25 Gbit/s, 2.5 Vp-p	
	Total Jitter	Typ. 8psp-p*	
	Waveform Distortion (0-peak)	Typ. ±25 mV ±10%@25 Gbit/s	
MU182020A-x13 (Variable Data Output	Amplitude Setting Error	0.5 to 3.5 Vp-p/2 mV Step Setting Error : ± 50 mV $\pm 17\%$ of Amplitude	
(0.5 to 3.5 Vp-p))	Offset Setting Error	-2.0 to $+3.3$ Voh, Min4.0 Vol/1 mV Steps Setting Error: ± 65 mV $\pm 10\%$ of Offset(Vth) \pm (Amplitude Setting Error/2)	
	Cross Point Setting Range	20 to 80%/0.1% Step	
	Tr/Tf	Typ.12ps(20 to 80%)@25 Gbit/s, 3.5 Vp-p	
	Total Jitter	Typ. 8psp ⁻ p*	
	Waveform Distortion (0-peak)	Typ. ±25 mV ±10%@25 Gbit/s	

Option Configuration	Signal Source	Operating Frequency Range Specification	Results
Clock Output (When MU182020A-x21 is not installed)	Amplitude Setting Error	Min. 0.3 Vp-p, Max. 1.0 Vp-p Min. 0.7 Vp-p, Max. 1.0 Vp-p (When MU182020A-x02 is installed)	
Clock Output (When MU182020A-x21	Amplitude Setting Error	0.5 to 2.0 Vp-p/2 mV Step Setting Error : ±70 mV ±17% of Amplitude	
is installed)	Offset Setting Error	-2.0 to $+3.3$ Voh, Min. -4.0 Vol/1 mV Step Setting Error: ± 65 mV $\pm 10\%$ of Offset(Vth) \pm (AmplitudeSetting Error/2)	
	Duty Setting Range	-25 to +25/1 Step(No Unit)	
Variable Data Delay	Phase Setting Range	-64000 to $+64000$ mUI/2 mUI Steps	
(When MU182020A-x30 or MU182020A-x31 is installed)	Accuracy	Typ. ±50 mUIp ⁻ p	

Table C.1–1 MU182020A (Cont'd)

Option Configuration	Signal Source	Operating Frequency Range Specification	Results
_	Operating Bit Rate	8.0 to 25.0 Gbit/s 8.0 to 28.0 Gbit/s (When MU182021A-x01 is installed)	
MU182021A-x10 (Variable Data Output	Amplitude Setting Error	0.25 to 1.75 Vp-p / 2 mV Step Setting Error : ±50 mV ±17% of Amplitude	
(0.25 to 1.75 Vp-p))	Offset Setting Error	 - 2.0 to + 3.3 Voh, Min4.0 Vol/1 mV Step Setting Error: ±65 mV ±10% of Offset(Vth) ± (AmplitudeSetting Error/2) 	
	Cross Point Tr/Tf	20 to 80% / 0.1% Step Typ.12ps(20 to 80%)@25 Gbit/s, 1.75 Vp-p	
	Total Jitter Waveform Distortion (0-peak)	Typ. 8psp-p* Typ. ±25 mV ±10%@25 Gbit/s	
	Data1/Data2 Skew	± 0.25 UI	

Table C.1-2 MU182021A

Option Configuration	Signal Source	Operating Frequency Range Specification	Results
MU182021A-x11 (Variable Data Output	Amplitude Setting Error	0.5 to 2.5 Vp-p/2 mV Step Setting Error : ± 50 mV $\pm 17\%$ of Amplitude	
(0.5 to 2.5 Vp-p))	Offset Setting Error	 -2.0 to +3.3 Voh, Min4.0 Vol/1 mV Step Setting Error: ±65 mV ±10% of Offset(Vth) ± (Amplitude Accuracy/2) 	
	Cross Point Setting Range	20 to 80% / 0.1% Step	
	Tr/Tf	Typ.12ps(20 to 80%)@25 Gbit/s, 2.5 Vp-p	
	Total Jitter	Typ. 8psp-p*	
	Waveform Distortion (0-peak)	Typ. ±25 mV ±10%@25 Gbit/s	
	Data1/Data2 Skew	±0.25 UI	

Table C.1–2	MU182021A (Cont'd)
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Option Configuration	Signal Source	Operating Frequency Range Specification	Results
MU182021A-x13 (Variable Data Output	Amplitude Setting Error	0.5 to 3.5 Vp-p/2 mV Step Setting Error : ± 50 mV $\pm 17\%$ of Amplitude	
(0.5 to 3.5 Vp-p))	Offset Setting Error	-2.0 to +3.3 Voh, Min4.0 Vol/1 mV Step Setting Error: ±65 mV ±10% of Offset(Vth) ± (AmplitudeSetting Error/2)	
	Cross Point Setting Range	20 to 80% / 0.1% Step	
	Tr/Tf	Typ.12ps(20 to 80%)@25 Gbit/s, 3.5 Vp-p	
	Total Jitter	Typ. 8psp-p*	
	Waveform Distortion (0-peak)	Typ. ±25 mV ±10%@25 Gbit/s	
	Data1/Data2 Skew	±0.25 UI Refer to MU182021A-x10 Data1/Data2 Skew	

Table C.1–2 MU182021A (Cont'd)

Option Configuration	Signal Source	Operating Frequency Range Specification	Results
Clock Output (When MU182021A-x21 is not installed)	Amplitude Setting Error	Min. 0.3 Vp-p, Max. 1.0 Vp-p Min. 0.7 Vp-p, Max. 1.0 Vp-p (When MU182021A-x02 is installed)	
Clock Output (When MU182021A-x21 is installed)	Amplitude Setting Error	0.5 to 2.0 Vp-p/2 mV Step Setting Error:±70 mV ±17%	
	Offset Setting Error	 -2.0 to +3.3 Voh, Min4.0 Vol/1 mV Step Setting Error: ±65 mV ±10% of Offset(Vth) ± (Amplitude Setting Error/2) 	
	Duty Setting Range	-25 to $+25/1$ Step(No Unit, Not independent)	
Variable Data Delay (When MU182021A-x30 or MU182021A-x31 is installed)	Phase Setting Range	-64000 to +64000 mUI/2 mUI Step	
	Accuracy	Typ. ±50 mUIp-p	

Table C.1–2 MU182021A (Cont'd)